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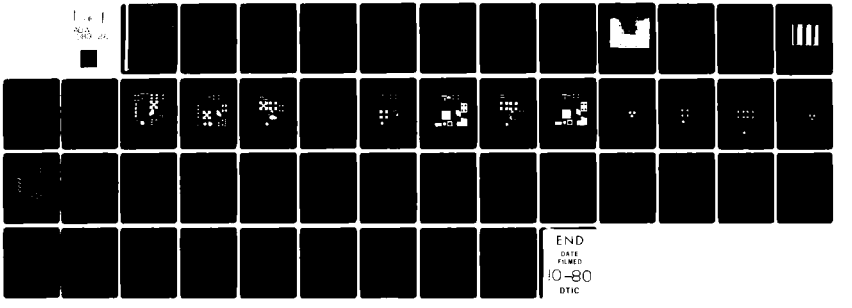

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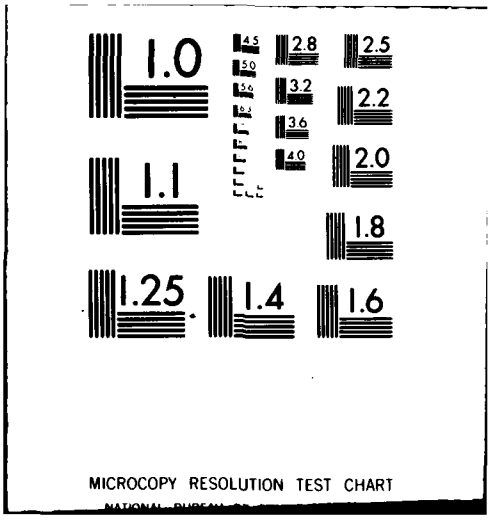
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ION IMPLANTATION OF WIDE BANDGAP SEMICONDUCTORS

K. V. Vaidyanathan, C. L. Anderson, H. L. Dunlap, and R. A. Jullens

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May 1980

Contract N00173–79–C–0028
Final Report
For period 15 December 1978 through 14 December 1979

Approved for public release; distribution unlimited.

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NAVAL ELECTRONICS SYSTEMS COMMAND
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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A089 026
	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) ION IMPLANTATION OF WIDE BANDGAP SEMICONDUCTORS	5. TYPE OF REPORT & PERIOD COVERED Final Report 15 Dec 78 - 14 Dec 79
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) K.V. Vaidyanathan, C.L. Anderson, H.L. Dunlap, R.A. Jullens	8. CONTRACT OR GRANT NUMBER(s) N00173-79-C-0028
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, California 90265	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 12, 58 C
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Electronics Systems Command Department of the Navy Washington, D.C. 20375	12. REPORT DATE May 80
	13. NUMBER OF PAGES 49
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Naval Research Laboratory 4555 Overlook Avenue, S.W. Washington, D.C. 20375	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs Ion Implantation
GaAs p-n Junctions
GaAs Bipolar Transistors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the development of a mask set and process technology for the fabrication of sequentially implanted p-n junctions and bipolar transistors in GaAs. Development of high-density implant masks is described. The electrical properties of the implanted p-n junctions are reported, and the dominant leakage current mechanism is identified.

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SECTION 1

INTRODUCTION AND SUMMARY

The primary objectives of this program are to study the electrical properties and carrier distributions in ion-implanted and annealed GaAs and to demonstrate the feasibility of forming planar, isolated p-n junctions by sequential implantation of donors and acceptors into semi-insulating GaAs. To fabricate such planar junctions, a selective area implantation process technology was developed. The required device isolation was achieved by exploiting the semi-insulating nature of Cr-doped GaAs.

To perform selective area implantation (required in a planar process), it is necessary to develop a suitable masking scheme such that none of the dopants penetrate undesired regions of the wafers. The simplest masking scheme would be to use a dielectric layer such as silicon oxynitride ($Si_xO_yN_2$) along with photoresist. However, to provide adequate masking for deep implants, excessively thick layers would be required. Such thick layers would lead to severe photolithographic problems, especially when fine pattern resolutions are required. During the early phase of this program, a masking scheme consisting of silicon oxynitride and germanium layers, both deposited by a plasma-enhanced process, was developed. The germanium layer had to be plasma etched, and the process had severe yield problems. Lift-off process are quite simple and result in excellent yield even when the pattern dimensions are micrometer sized. A lift-off process was developed to use Cr-Au as an implant mask. This process is described in detail in Section 2.

In designing the implants for p-n junction fabrication, it is necessary to know the electrical properties of the doped layers. In particular, the lowest and highest concentrations of dopants that can be activated in Cr-doped GaAs has to be known. We performed experiments to determine these parameters. It is also necessary to evaluate the electrical activation and the carrier mobilities on the device wafer itself. We designed a versatile mask set to fabricate test structures, including

van der Pauw patterns for Hall-effect measurements, Schottky barriers for capacitance-voltage (C-V) measurements, and p-n junctions with different areas. The p-n junctions were characterized by measuring the current-voltage (I-V) characteristics both in the forward and reverse directions and the breakdown voltage of the devices. A detailed study showed that surface leakage is the dominant leakage mechanism in these planar diodes. The results of the electrical evaluation are discussed in Section 3.

SECTION 2

PROCESS DESIGN

The major aim of this program is to develop a reliable process technology for fabricating planar, fully ion implanted, isolated p-n junctions and bipolar transistors. Since these devices are to be isolated, we decided early during this reporting period to exploit the semi-insulating nature of the Cr-doped GaAs substrates to provide the required isolation between the devices. This section discusses experiments performed to develop a localized implantation capability and the mask set used to fabricate these devices.

A. LOCALIZED IMPLANTATION STUDIES

Before planar isolated p-n junctions can be formed, a masking scheme must be developed that will prevent ions from penetrating regions where they are not wanted. A dielectric layer such as SiO_2 or Si_3N_4 along with a layer of photoresist formed by conventional lithography could be used as a simple mask. The major problem with this approach is the rather low stopping power of both layers. This is especially a problem when one wishes to form deep layers, and those as required for vertical bipolar transistors. Masking deep layers would require using excessively thick oxide or PR layers. The use of such thick films frequently results in poor pattern definition. We believe that the use of thin films of a denser material will alleviate this problem and that such a thin film will serve adequately as an implant mask.

We have developed a process that utilizes plasma-deposited layers of silicon oxynitride and germanium. Conventional photolithographic techniques are used, and the germanium layer is plasma etched. An SEM photograph of a processed sample is shown in Figure 1. The sample has a strip $\sim$1.5 μm wide where the Ge has been etched off; the nearly vertical sidewall is visible. The yield of this process is, however, poor. The poor yield coupled with the necessity of using relatively thick Ge layers makes it attractive to use heavy metals such as Au, W, or Au-Cr for masking.

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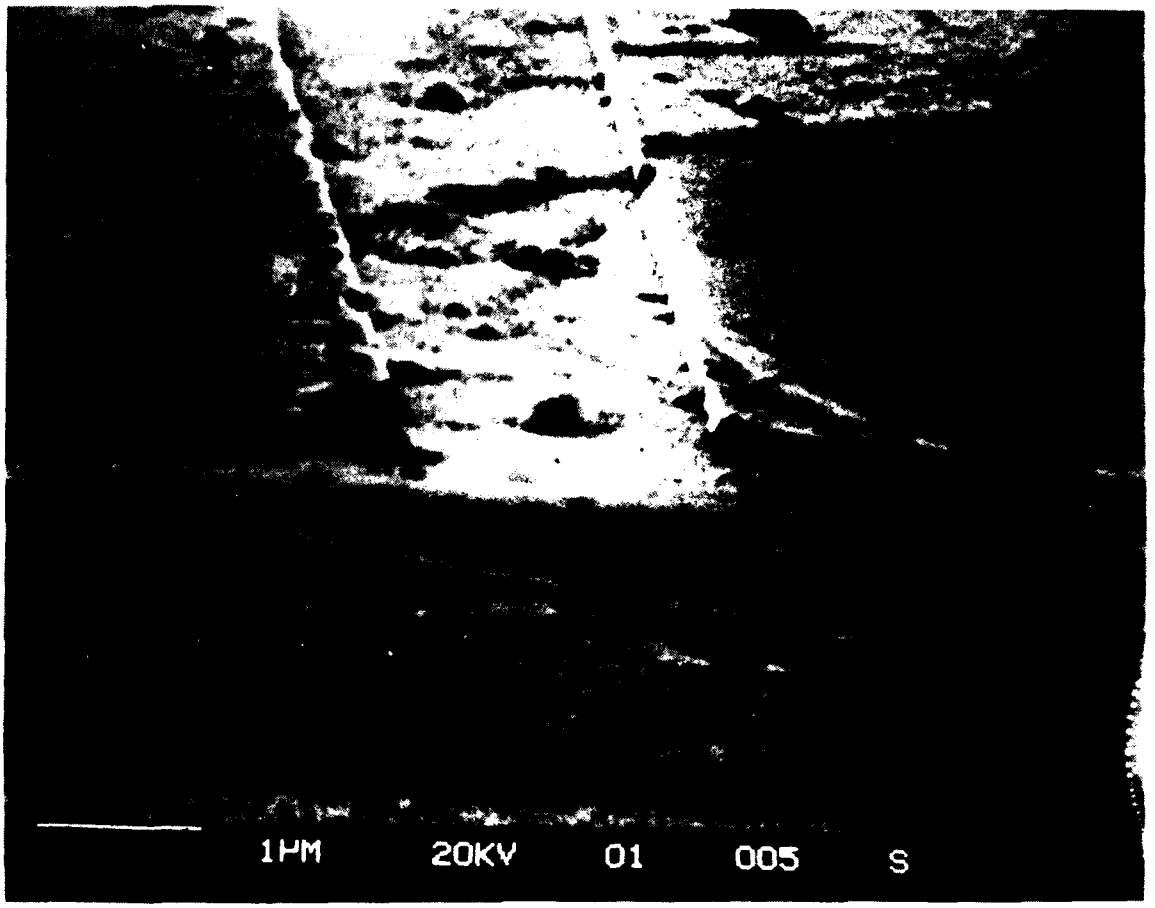

Figure 1. SEM photograph of a 1.5-μm-wide stripe formed by plasma etching of Ge deposited over silicon oxynitride on GaAs. The silicon oxynitride-germanium layer will be used as an implant mask.

Severe problems were encountered, however, in lifting Cr-Au or Au when the metal was directly evaporated onto a thin dielectric layer. The use of an intermediate layer of Al during the lift-off procedure resulted in an acceptable yield from the process. The process is described below, and the major processing steps are shown in Figure 2.

First, the wafer is cleaned with solvents and etched in an $H_2O:H_2O_2:NH_4OH$ (480:4:10) etch for 5 min. This removes ∿1 μm from the surface while maintaining a smooth, shiny appearance. A silicon oxynitride film, ∿400 Å thick, is then deposited on the wafer at 350°C by the plasma-enhanced deposition (PED) process using the LFE PND-301 system. A layer of photoresist (Shipley 1350J) is spun on the oxide layer followed by 3000 Å of Al. Following a photoresist and exposure step using an appropriate light field mask, the Al layer is etched in an $H_3PO_4:CH_3COOH:HNO_3:H_2O$ (76:6:3:15) etch at ∿40°C for ∿1.5 min. Following the Al etch, the underlying photoresist layer is exposed, typically for 1.5 min, to ensure considerable undercutting of the resist. This is followed by evaporation of ∿200 Å of Cr and then of Au to a total thickness of ∿5000 Å. The process is completed by lift-off of the Cr-Au composite. The process is highly reproducible and results in acceptable yield. SEM micrographs of the wafer after going through the process are shown in Figure 3.

B. PHOTOMASK DESIGN

We have designed a versatile mask set for this program. This section, with the aid of accompanying photographs, describes it in detail.

The mask set allows us to perform three localized sequential implants, as is required for fabricating fully ion implanted planar isolated bipolar transistors. The mask set has provisions for making Hall-effect and C-V evaluations of each implanted layer. The process can thus be evaluated at every step. This will help in correlating device parameters with process variables. Diodes with 25, 50, 100, 200, and 400 μm diameters can be fabricated and formed either by the base-collector or the base-emitter implants. Field-effect transistors (FETs)

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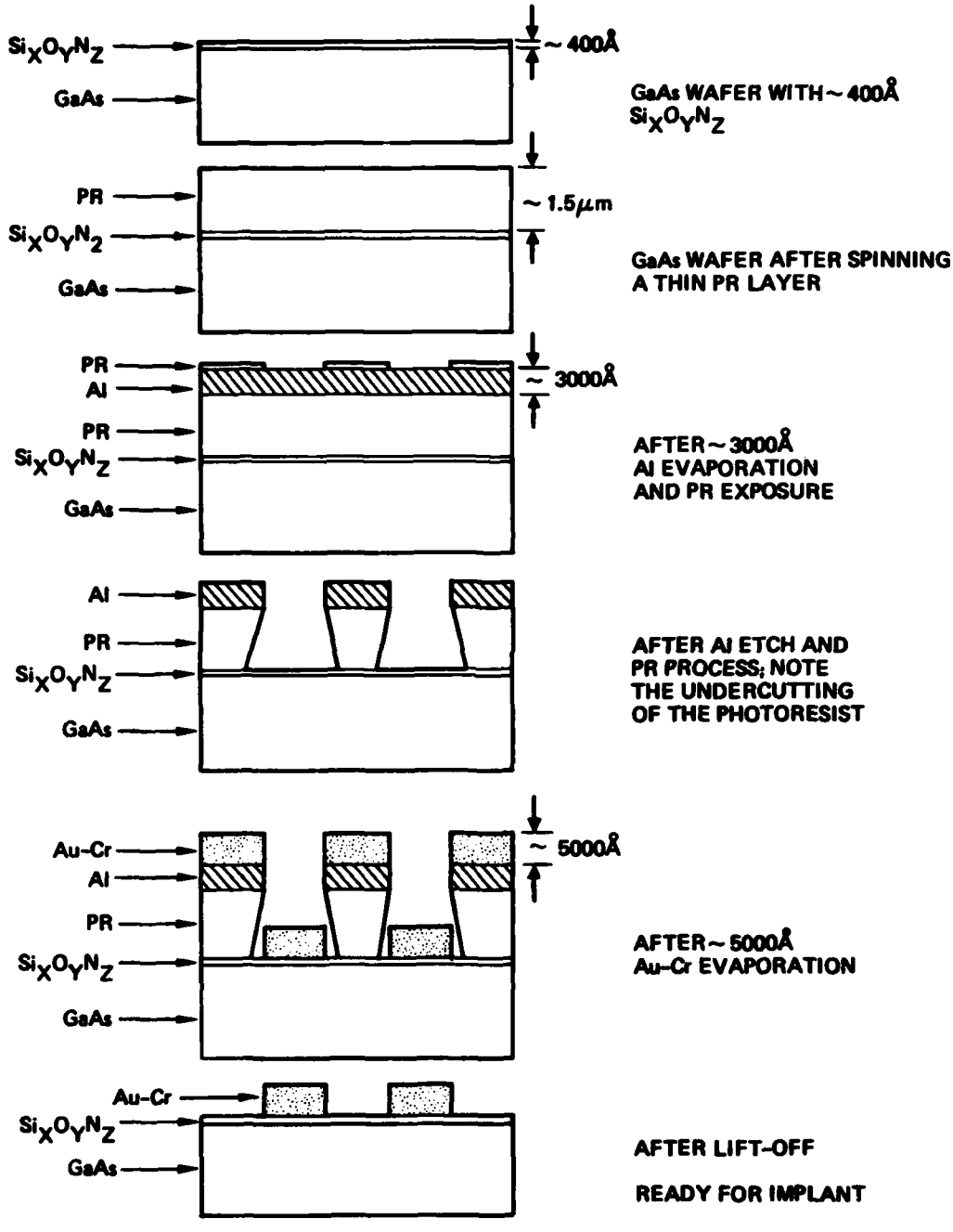

Figure 2. Flow chart of the processing steps involved for masked implants in GaAs.

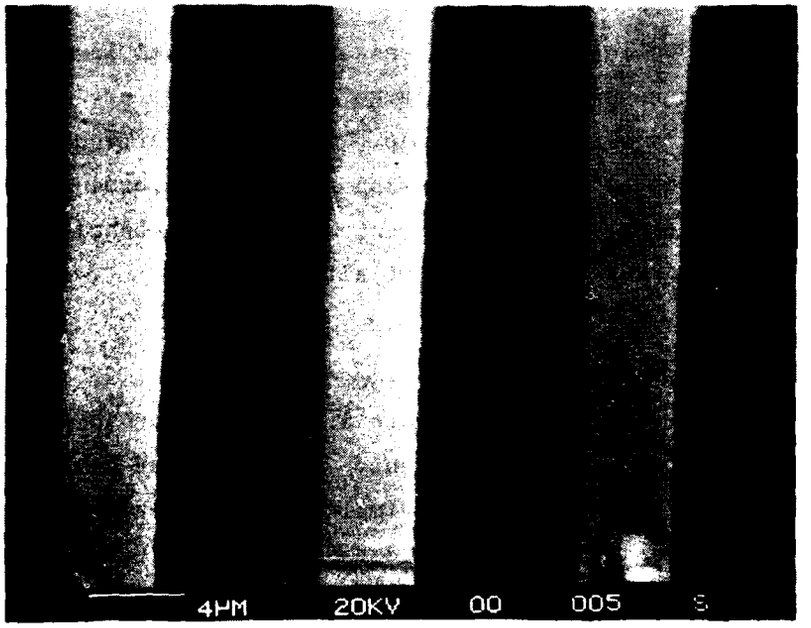

Figure 3. SEM micrograph of wafer after going through the lift-off process.

can be fabricated with this set as well as patterns for evaluating the contact resistance of Ohmic contacts. There is also a pattern for checking for any surface conversion effects by evaluating the resistance between adjacent implanted regions. The masks are described below in detail.

1. Level 0

The mask shown in Figure 4 represents the initial level in the mask set. The pattern consists of one large etched region per chip and is useful for visually aligning the chip. It will be particularly useful if a technique such as laser processing is used for forming Ohmic contacts. There is also another alignment mark; it is etched into GaAs and will serve as a marker for subsequent alignments.

2. Level 1

The level 1 mask, shown in Figure 5, is the first operational mask and will be used for collector implants. Regions that are clear in this mask as shown are regions where the implant mask material is present. Elements in this mask include a Van der Pauw Hall pattern, a segment for C-V measurements, and collector implants for transistors and diodes.

3. Level 2

The level 2 mask, shown in Figure 6, serves as the base implant mask for bipolar transistors. This level also includes selective implant areas for Hall and C-V evaluations.

4. Level 3

The level 3 implant mask, shown in Figure 7, serves as an emitter implant mask. Note that this level also allows for increasing the surface concentration in the Ohmic-contact regions for the collector and in the C-V analysis segments.

After the emitter implant, the sample is ready to be annealed with or without an encapsulant.

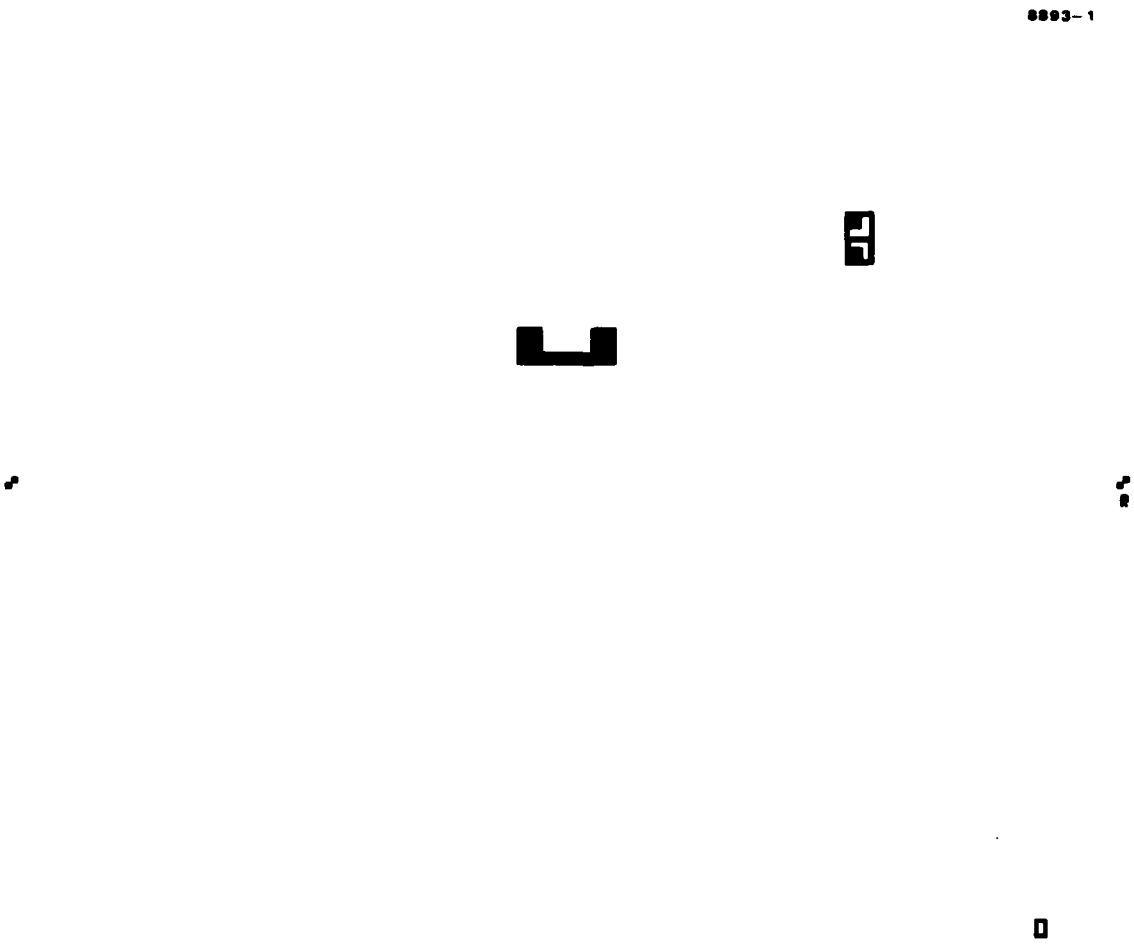

Figure 4. Level 0 mask. This will be used for etching alignment marks in the substrate.

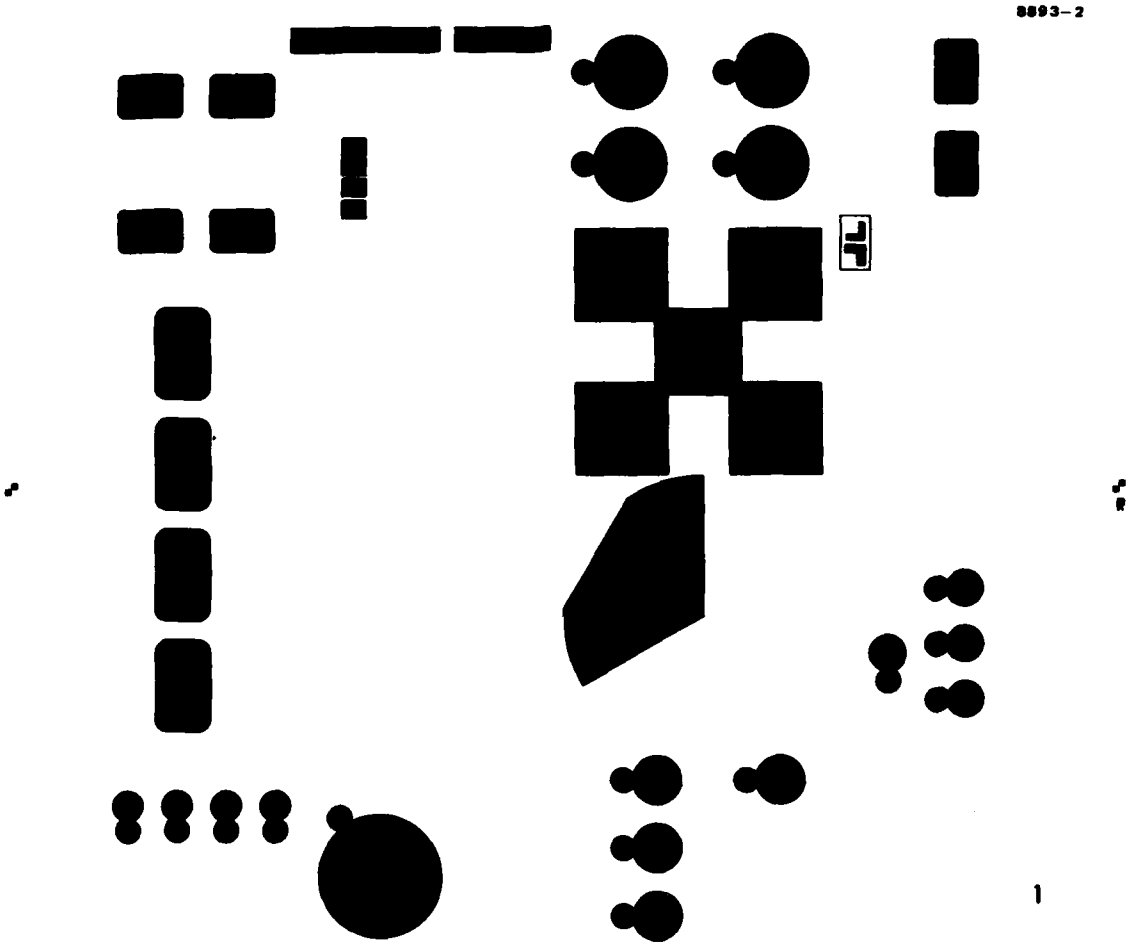

Figure 5. Level 1 mask. Implantation mask for collector-implants. The dark regions in the mask will receive the collector implant.

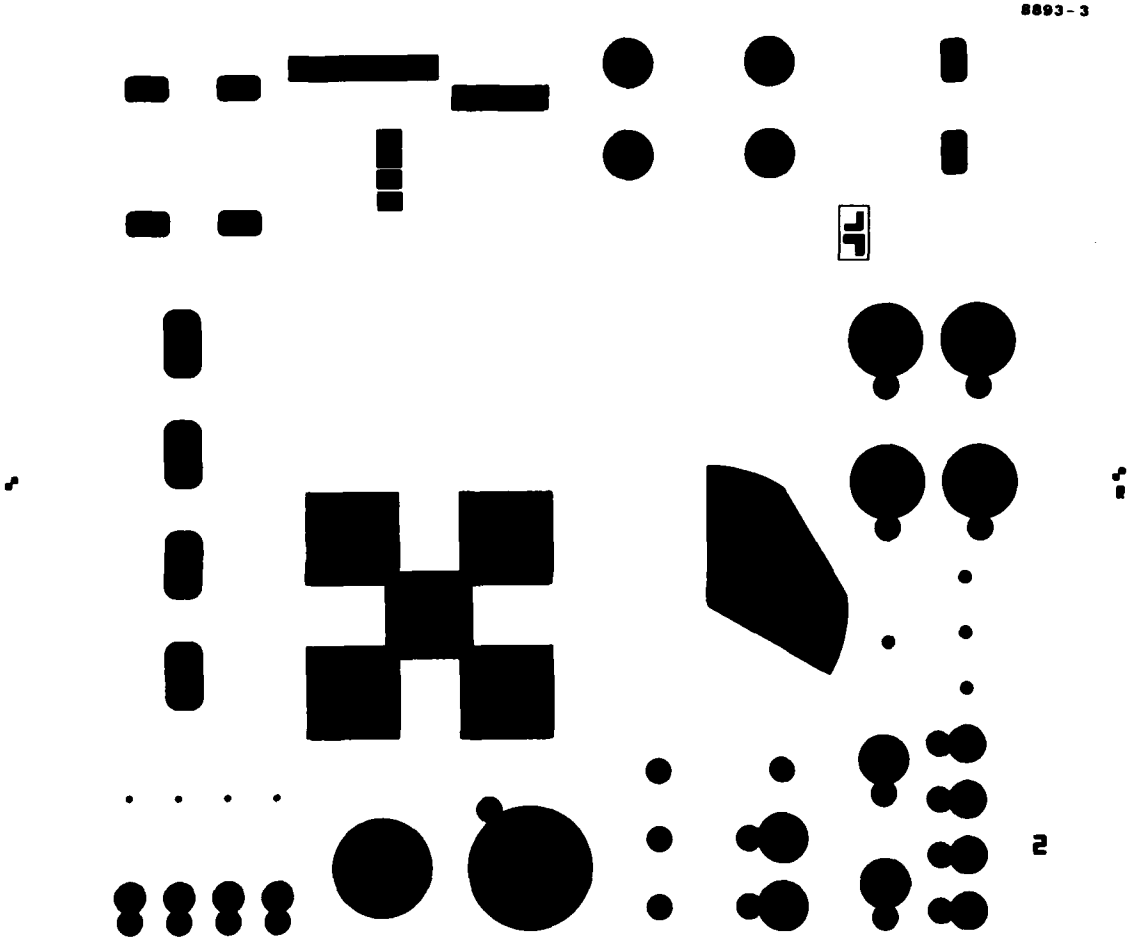

Figure 6. Level 2 mask. Base implant mask.

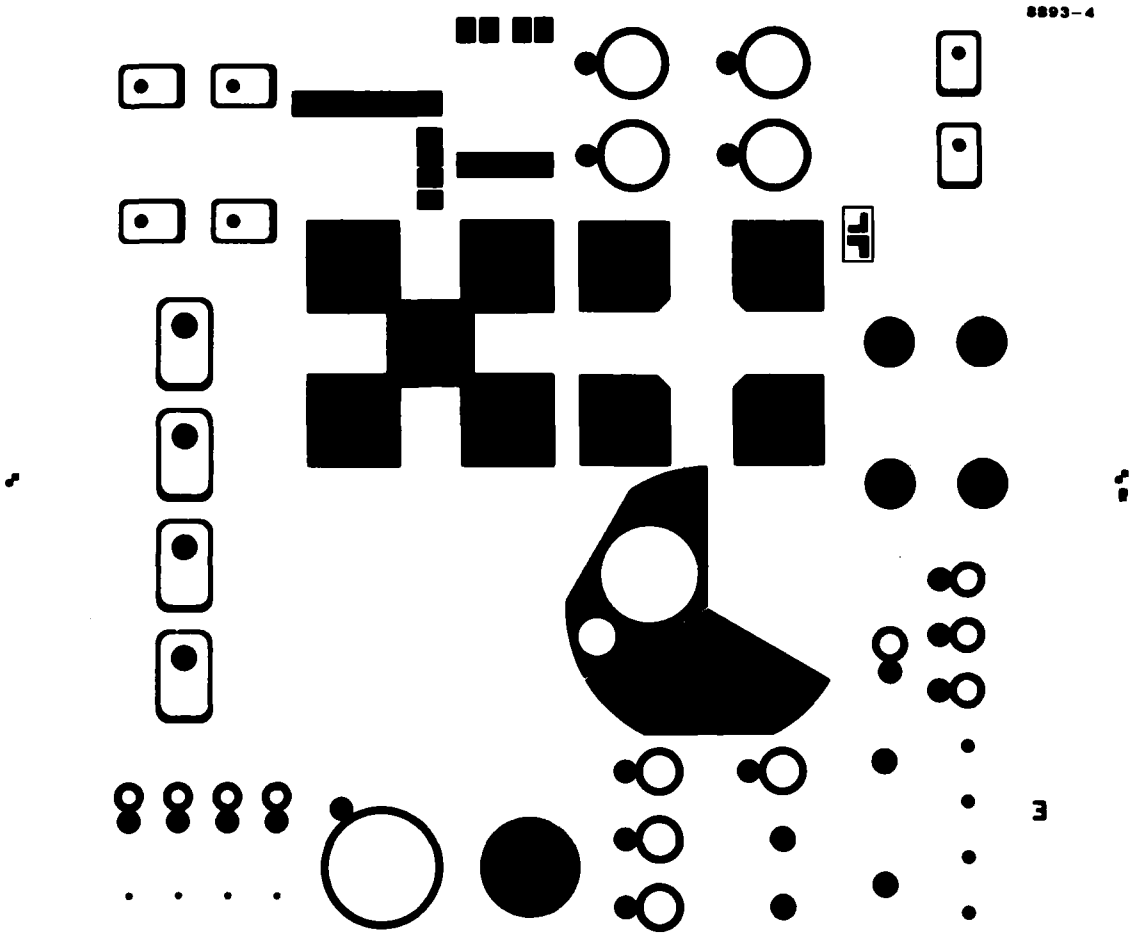

Figure 7. Level 3 mask. This will be used for emitter and collector contact region implant.

5. Levels 4 and 4'

The level 4 mask, shown in Figure 8, defines the Ohmic-contact metalization in regions that have received base implants. These regions can be defined either by lift off or chemical etching. If chemical etching is used in subsequent steps, mask 4' (Figure 9) will be used to protect the base contact metal.

6. Levels 5 and 5'

The level 5 mask (Figure 10) defines the metalization to regions which have received collector and emitter implants. Mask 5' (Figure 11) assures that these metalized regions are protected during subsequent processing if the metal is chemically etched off in Level 6. Also, during steps 4 and 5, the contact evaluation patterns are defined. This will allow us to evaluate the nature of the Ohmic contacts.

7. Level 6

This mask (Figure 12) allows us to define the Schottky barriers for performing C-V evaluations. There are two Schottky diodes with different areas. Also, the gate metalization is defined for forming the FETs. Levels 4, 5, and 6, along with 4' and 5', are designed to take into account that different metalizations have to be used for making Ohmic contacts to p and n regions and for forming a Schottky barrier.

8. Level 7

In fabricating sealed junctions, the junctions must be passivated with a suitable glassy dielectric. After this layer has been deposited, Mask 7 (Figure 13) can be used to open holes for making contact to the base metal.

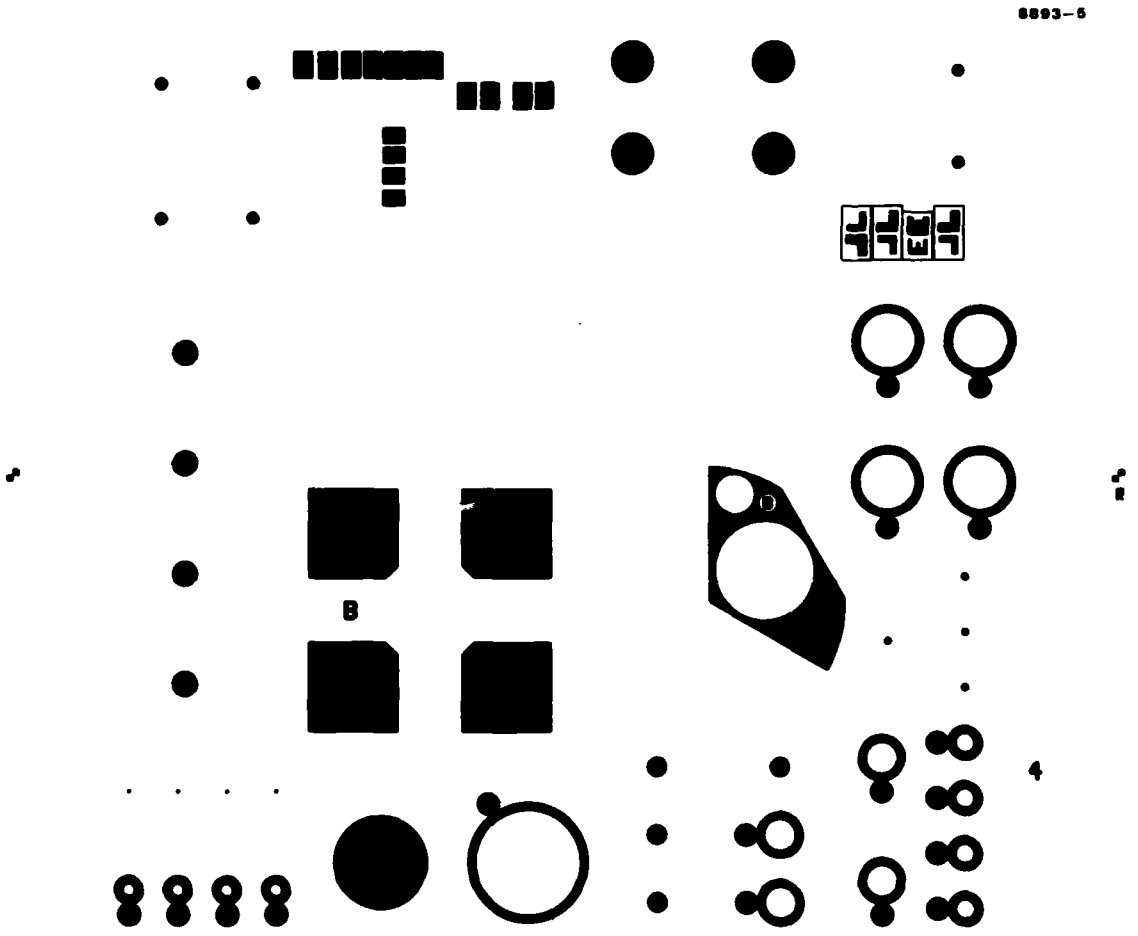

Figure 8. Level 4 mask. This will be used for contact metalization to base regions.

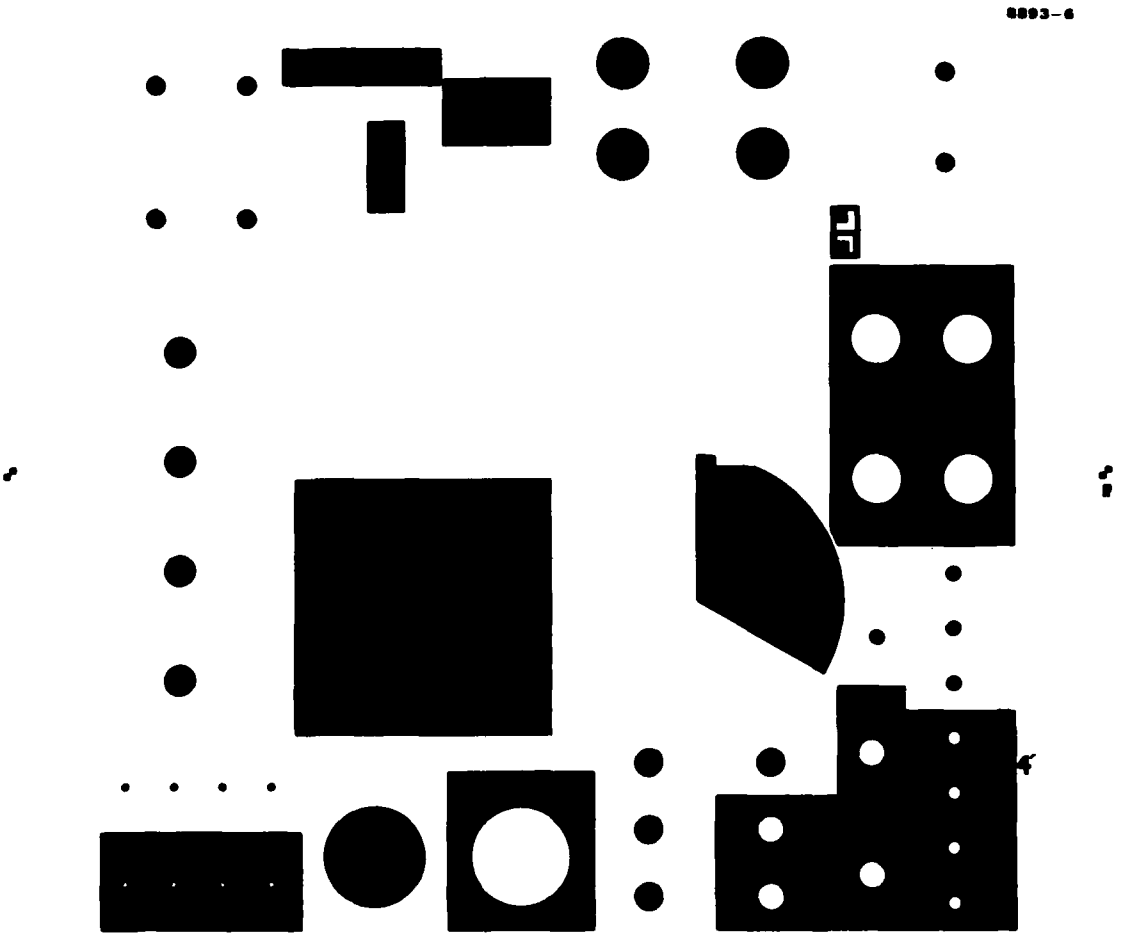

Figure 9. Level 4' mask. To protect base metalization during subsequent processing, especially if chemical etching is used to define the metalization pattern.

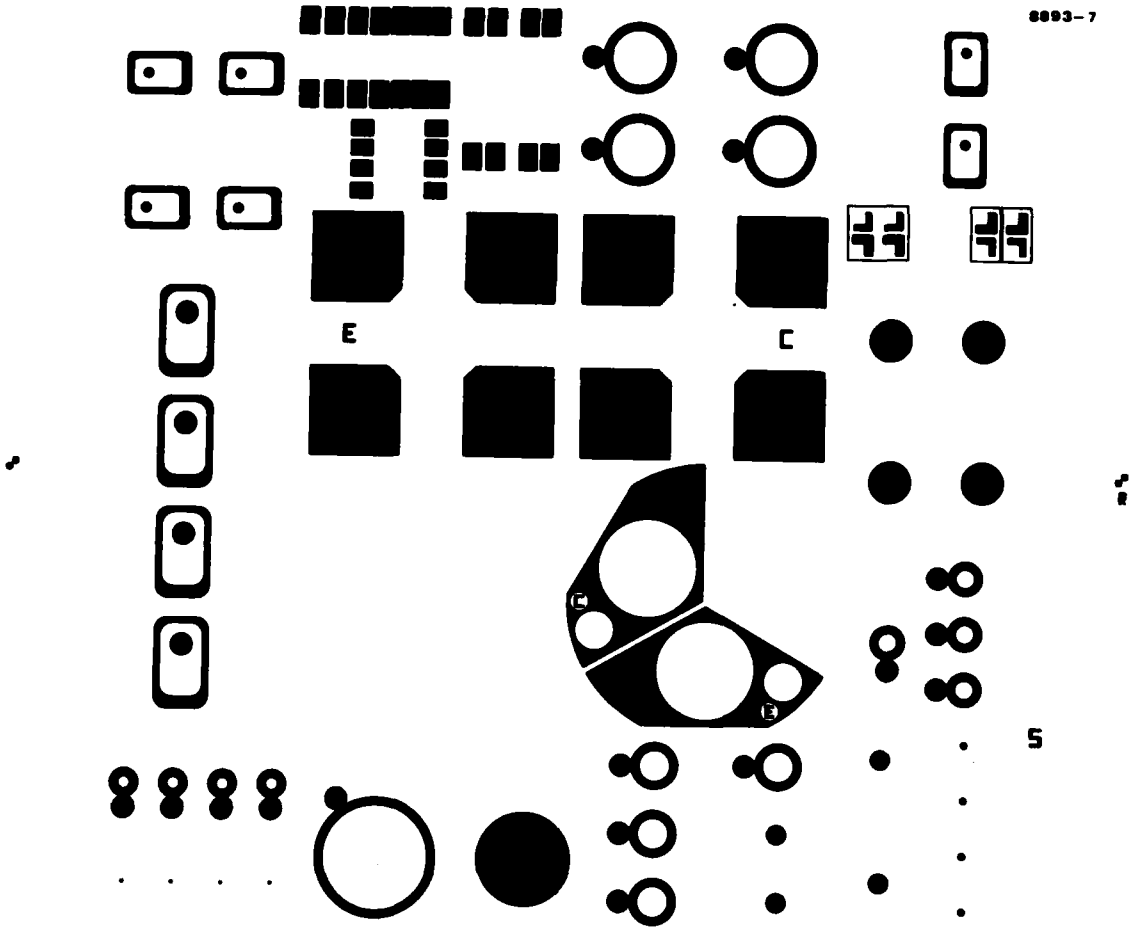

Figure 10. Level 5 mask. Collector-emitter metalization mask.

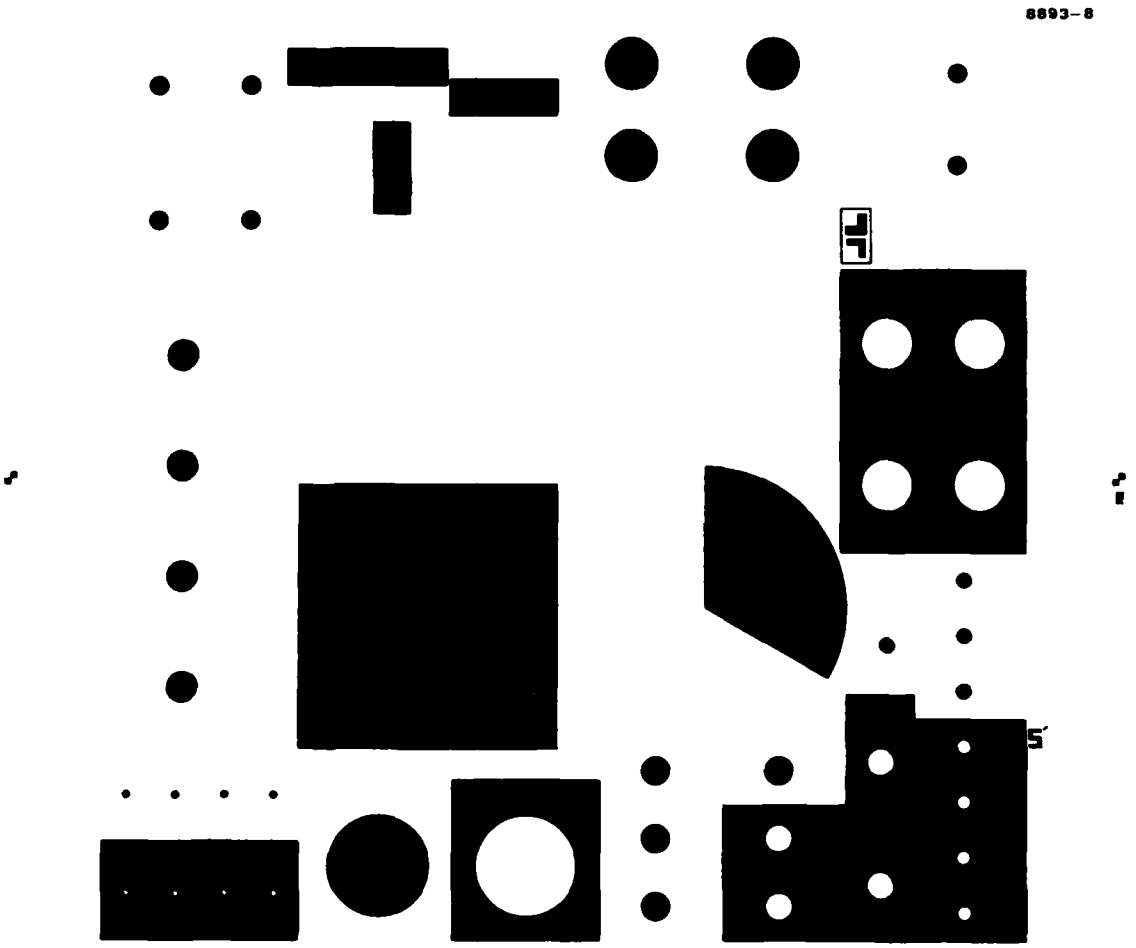

Figure 11. Level 5' mask. Useful for protecting collector-emitter metalizations during subsequent processing.

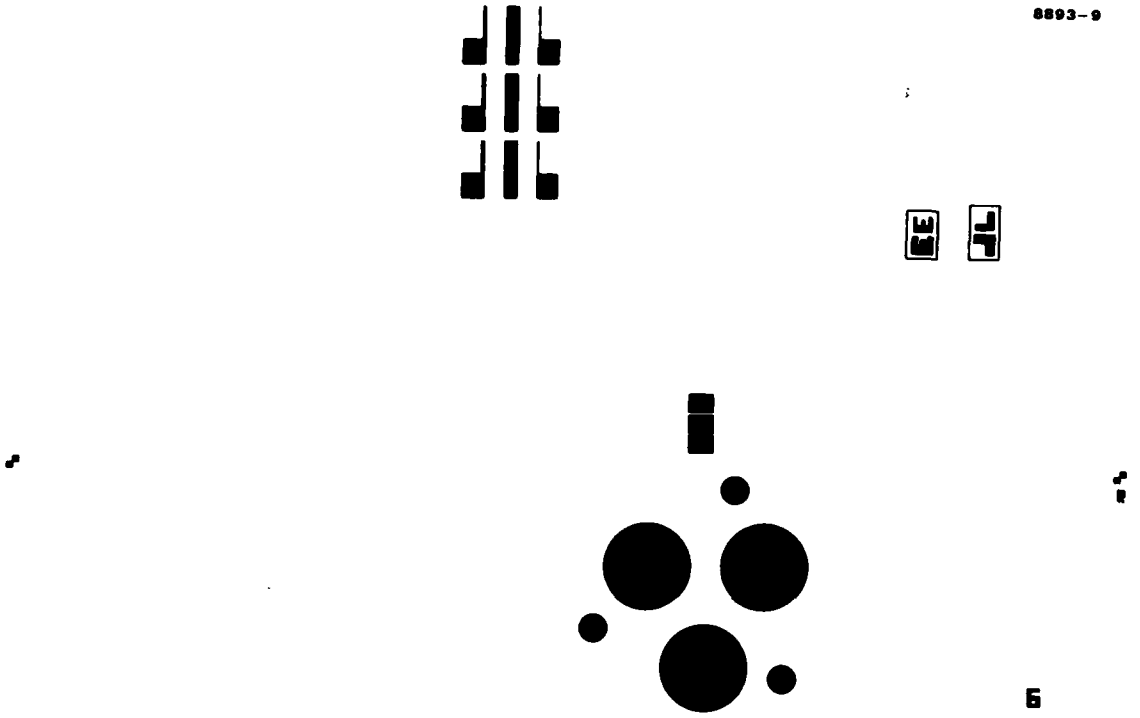

Figure 12. Level 6 mask. Used for forming Schottky-barrier metalization.

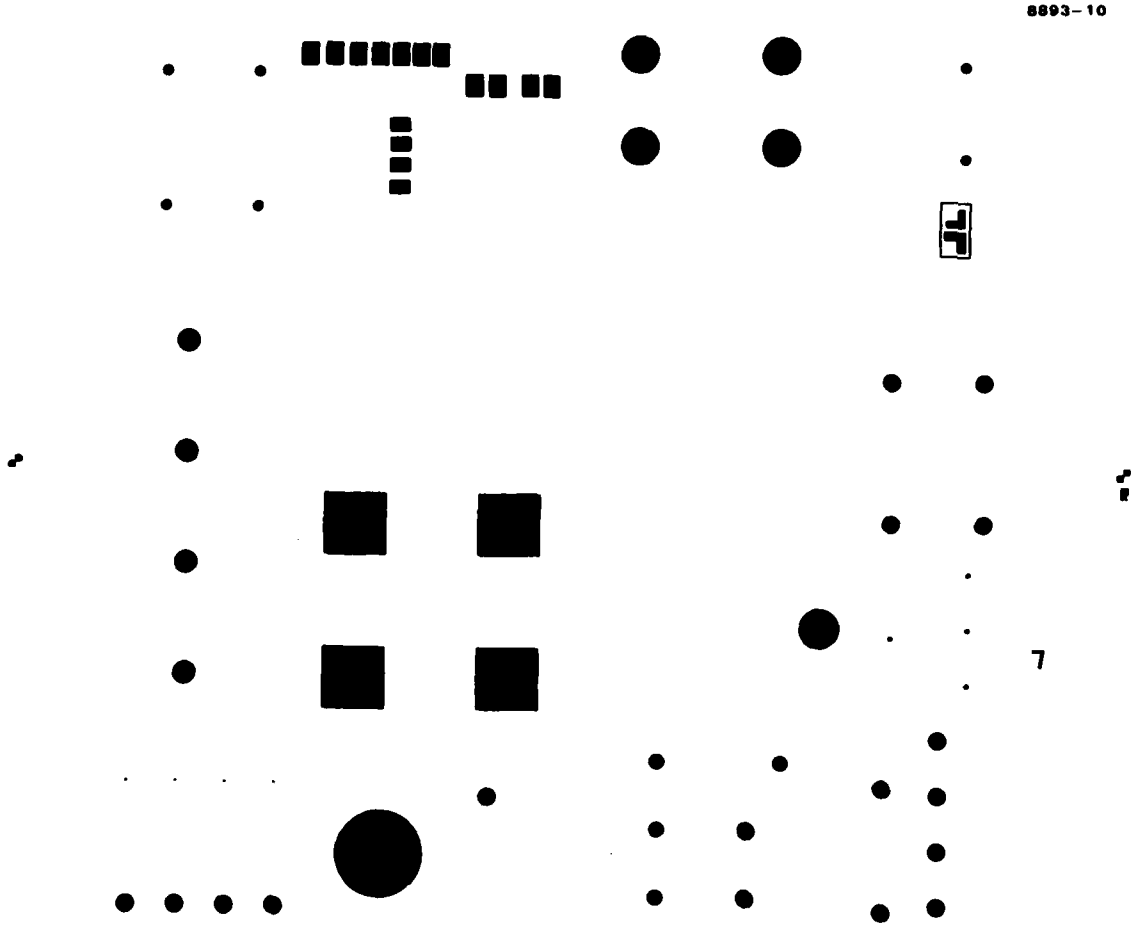

Figure 13. Level 7 mask. Used for opening holes in the glassy dielectric passivation layer to contact the base metalization.

9. Levels 8 and 9

The masks used in levels 8 and 9 (Figures 14 and 15) are used to open holes in the insulator to make contacts with the emitter/collector metalization and to the Schottky-barrier metalization, respectively.

10. Level 10

This mask (Figure 16) allows the various metalized regions to be brought to the bonding pads.

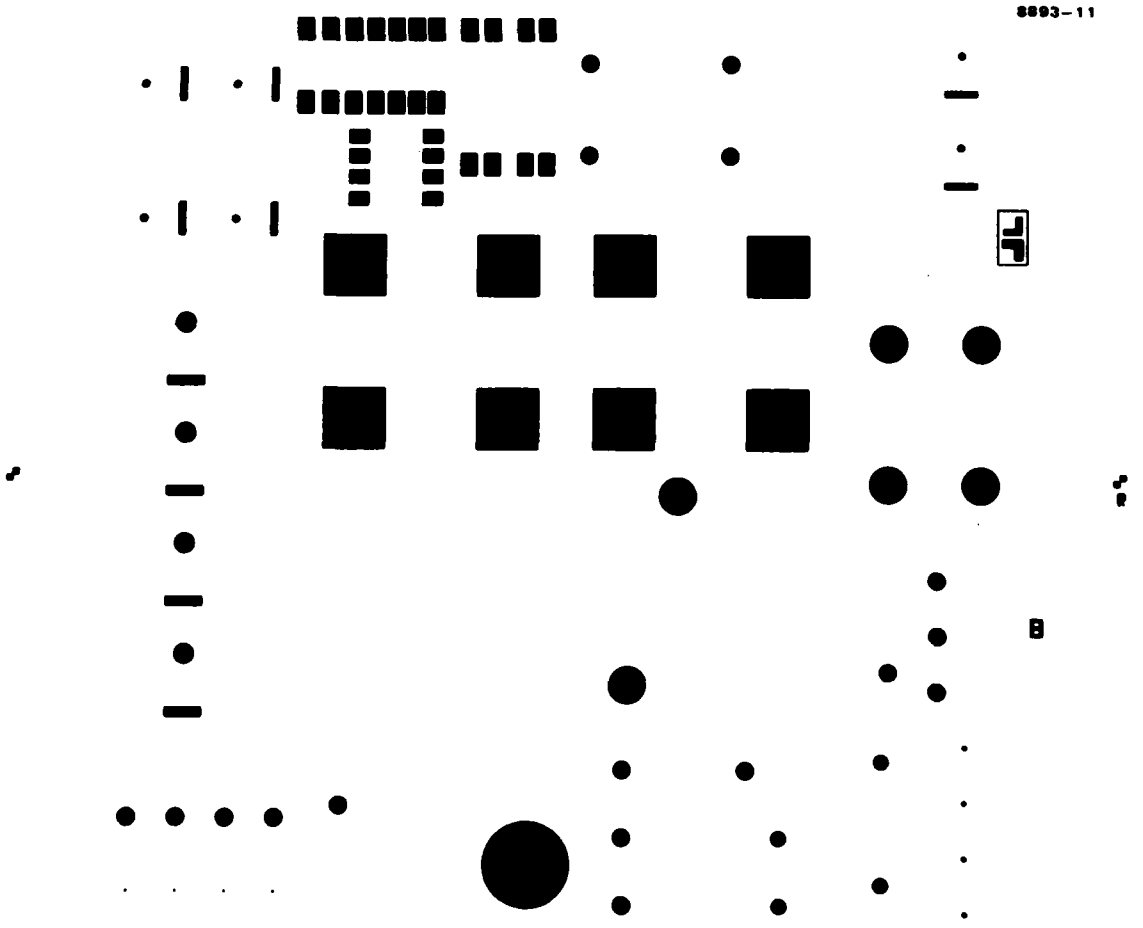

Figure 14. Level 8 mask. Used for forming the dielectric to emitter-collector metalizations.

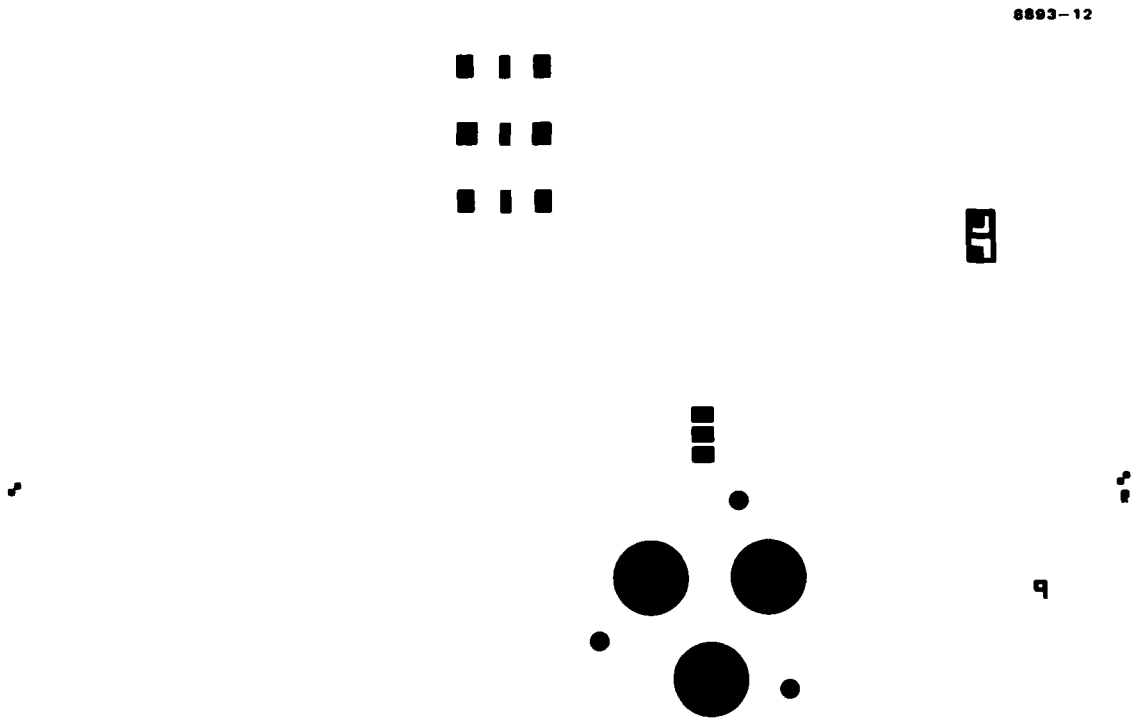

Figure 15. Level 9 mask. Used to open holes in the dielectric to the Schottky-barrier metalization.

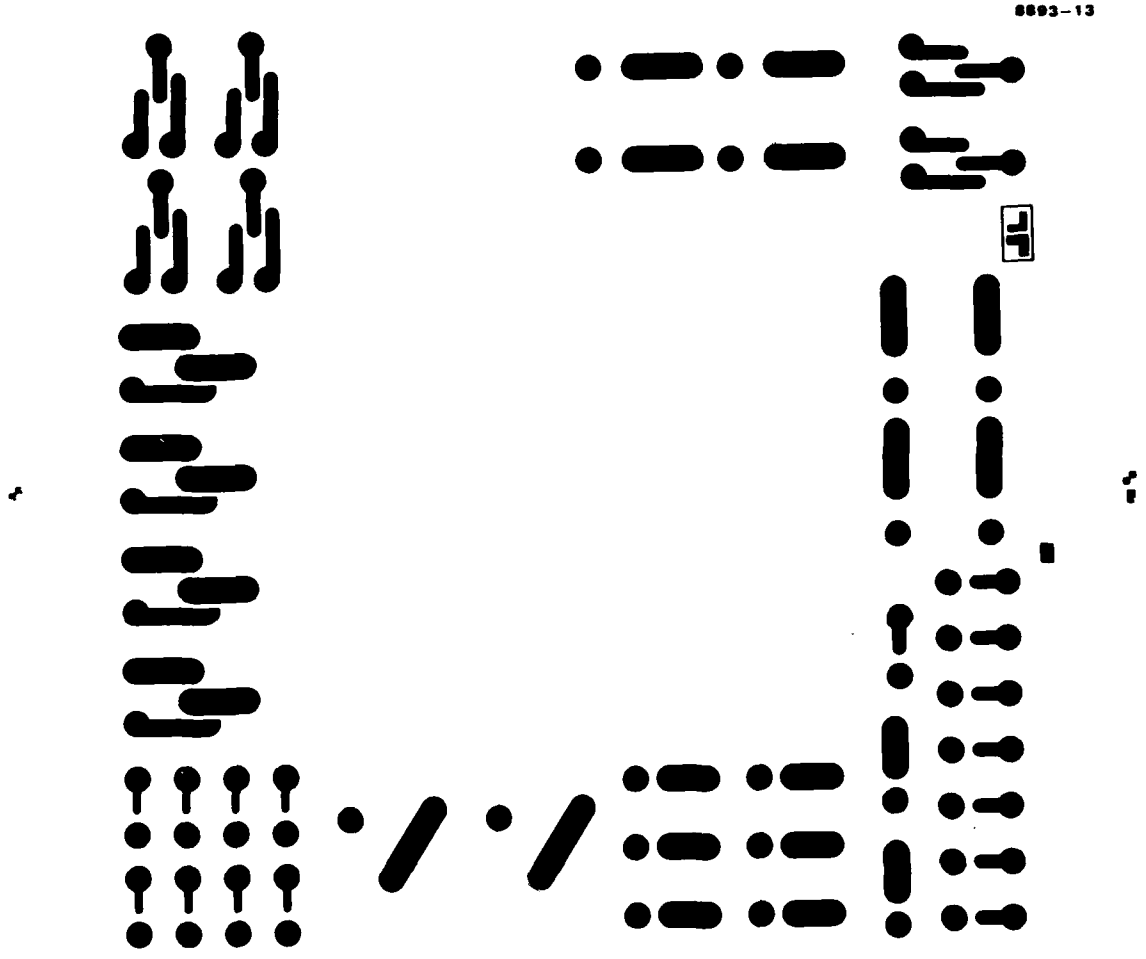

Figure 16. Level 10 mask. This mask will allow us to connect the various metalized regions to bonding pads.

SECTION 3

ION IMPLANTATION AND ELECTRICAL EVALUATION STUDIES

This section describes the implantation and electrical evaluation of the implanted layers and the p-n junctions. Preliminary experiments on implantation performed in the early phase of this work are described in Section 3.A. Section 3.B discusses the electrical evaluation of p-n junctions formed in semi-insulating GaAs by sequential ion implantation of Se and Be.

A. PRELIMINARY ELECTRICAL EVALUATION OF IMPLANTED LAYERS

To design ion implanted p-n junctions, it is necessary to know the apparent electrical activation of the implanted species, the carrier mobility, and the carrier distribution in the implanted layers. All of these parameters are influenced by several factors, including the annealing environment and the encapsulant used. Consequently, the electrical properties of Be- and Se-implanted layers were studied.

Be is an efficient acceptor dopant and, for concentrations at or below 3 to 5 x 10^{18} cm^{-3}, the Be distribution after annealing is not significantly different from the as-implanted distribution.[1] This provides an upper limit of 1 to 2 x 10^{18} cm^{-3} on the maximum Be concentration that can be used without risking having severe redistribution effects take place. To estimate the minimum acceptor concentration that can be efficiently activated, a multiple energy implant scheme was designed and the doses varied to achieve Be concentrations ranging from 3 x 10^{16} cm^{-3} to 1 x 10^{17} cm^{-3}. The theoretically calculated distribution is shown in Figure 17. Table 1 shows the electrical activation data obtained from samples annealed at 800°C using our patented melt controlled ambient technique (MCAT).[2] Figure 18 shows the carrier concentration profile as measured by C-V measurements on a sample implanted to a uniform concentration of 10^{17} cm^{-3} and annealed at 800°C for 30 min.

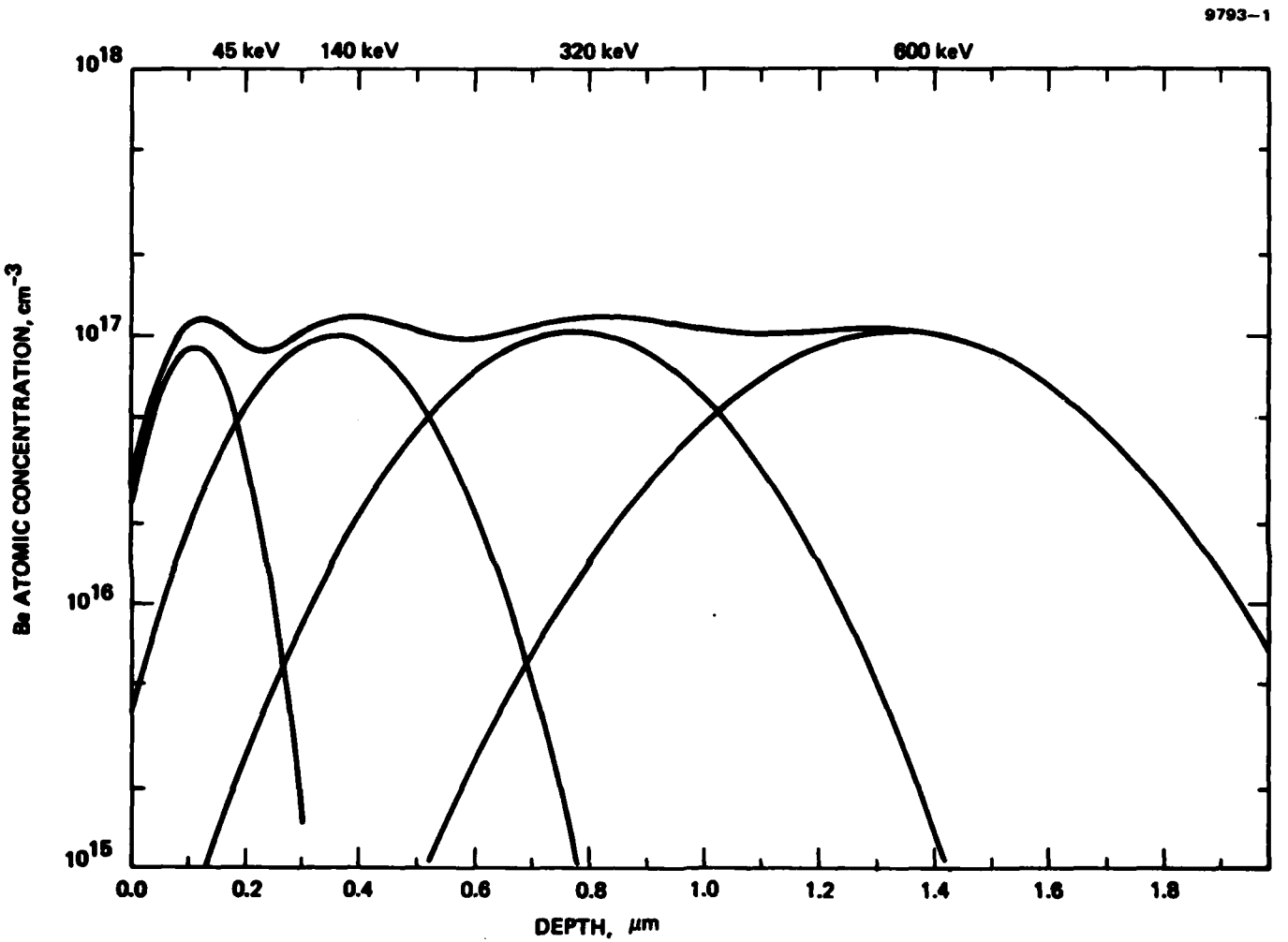

Figure 17. Theoretical design of a four-energy Be implant, showing the four Gaussian single-energy implant profiles and their summation.

Table 1. Electrical Properties of Low-Concentration Be-Implanted Layers. MCAT Annealed at 800°C

Desired Concentration, cm^{-3}	Sheet Resistivity, Ω/□	Hole Mobility, $cm^2 V^{-1} sec^{-1}$	Apparent Electrical Activation, %
10^{17}	1630 ± 90	230 ± 8	94 ± 8
5×10^{16}	6270 ± 1700	235 ± 14	50 ± 10
3×10^{16}	44,000	170	∿16

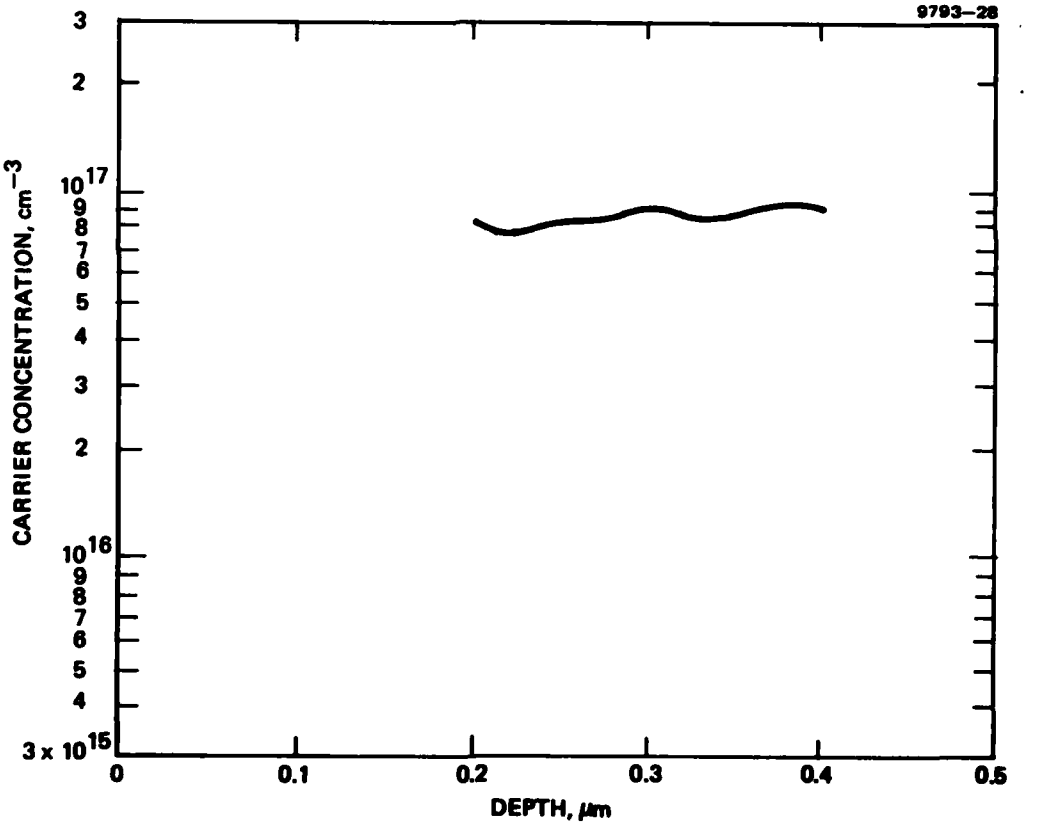

Figure 18. Carrier concentration profile obtained by C-V measurements from a Be-implanted sample and annealed at 800°C, 30 min. The as-implanted calculated profile is shown in Figure 17.

It is well known that Se is a well-behaved donor in GaAs and can be efficiently activated. Previous work performed at this and other laboratories has demonstrated that low fluence, room-temperature Se implants can be effectively activated. However, to achieve high donor concentrations using Se, elevated temperature implants will be required. For ease in processing, we decided to fabricate a p^+-n structure by sequential implantation of selenium and beryllium. The electrical properties of the implanted layers and the current-voltage characteristics of the junction devices are described in the following section.

B. p-n JUNCTION FABRICATION AND ELECTRICAL EVALUATIONS

After developing the selective masking technology, three different wafers of Cr-doped, semi-insulating GaAs were subjected to sequential implants to fabricate p-n junctions. A deep n-type layer was first implanted, followed by a shallower p-type layer. For n-type doping, Se was used as the dopant of choice, while for p-type doping, Be was used as the dopant. To make the analysis easier, a multiple energy implant scheme was designed to provide a uniform concentration for the n-type layer. Table 2 provides the implant energies and fluences used for the three wafers designated NRL-A, B, and C. In all cases, the Be implant energy and dose were kept constant at 25 keV and 1.5×10^{13} cm^{-2}, respectively. The samples were annealed at 850°C for 30 min with silox encapsulant. Figure 19 shows the impurity profiles of implanted Be and Se obtained by secondary ion mass spectrometry (SIMS) from wafer C. Ohmic contacts to the n-type layers were formed by alloying evaporated Au-Ge-Ni, while contacts to p-type layers were formed by alloying evaporated Ag-Mn contacts. The alloying was performed at ∿350°C for 1 min in flowing forming gas. Hall-effect measurements were performed on appropriate Van der Pauw patterns. The data from n-type implanted layers are shown in Table 3, while data from p-type layers are shown in Table 4. The implants were performed through ∿400 Å of $Si_xO_yN_z$ deposited by a PED process. We estimated that ∿20% of the implanted ions (both Be and Se) come to rest within the silicon oxynitride layers. Using this

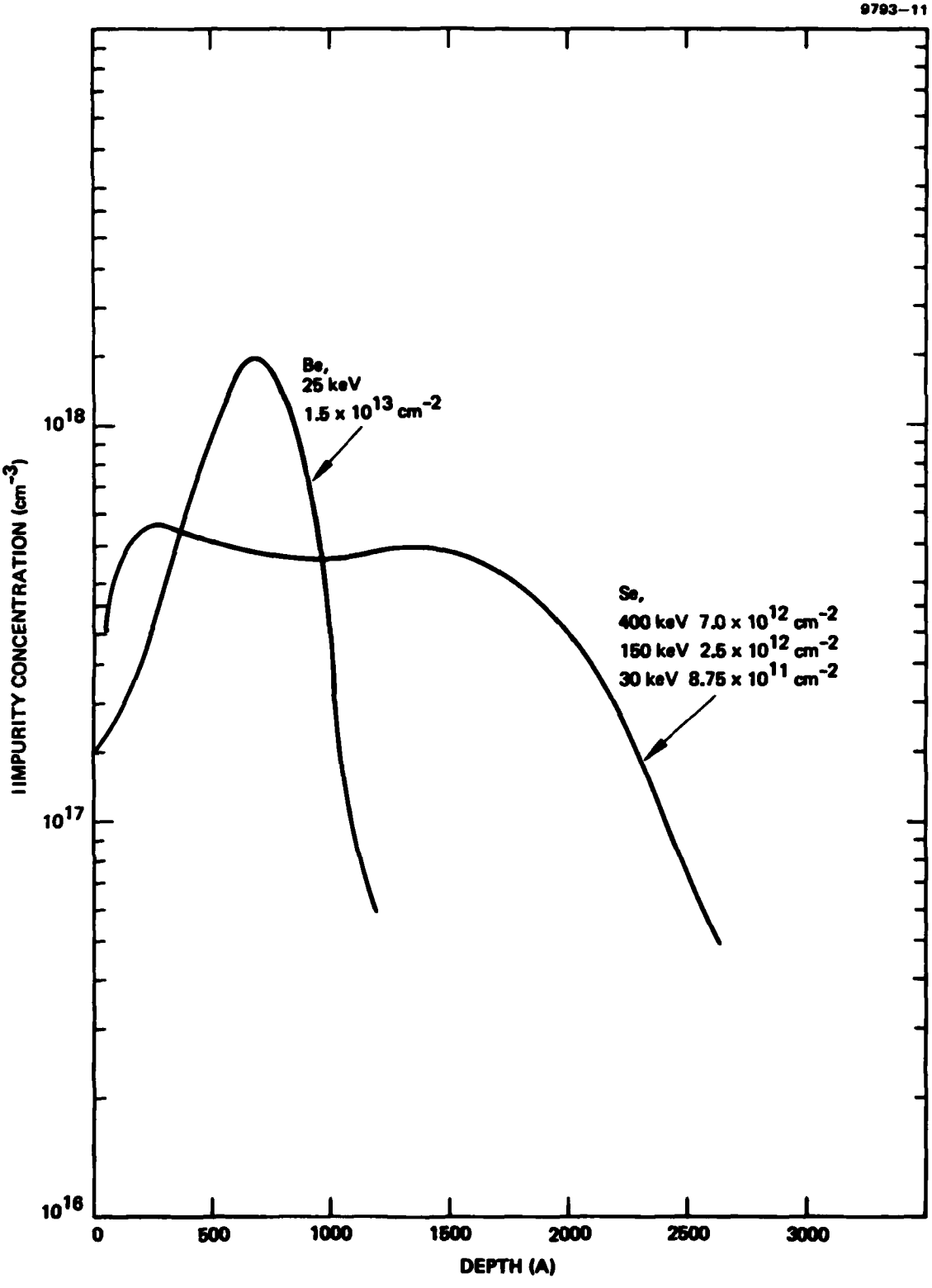

Figure 19. Impurity profiles of Se and Be obtained from SIMS measurements on wafer NRL-C.

Table 2. Se Implant Energies and Fluences Used to Simulate Uniformly Doped n-Type Layers

Wafer	Dopant Concentration, cm^{-3}	Ion Dose in cm^{-2} at		
		400 keV	125 keV	30 keV
A	2×10^{17}	2.8×10^{12}	1×10^{12}	3.5×10^{11}
B	4×10^{17}	5.6×10^{12}	2×10^{12}	7×10^{11}
C	5×10^{17}	7.0×10^{12}	2.5×10^{12}	8.75×10^{11}

Table 3. Electrical Properties of Se-Implanted Layers Annealed at 850°C for 30 min

Wafer	Sheet Resistivity, Ω/□	Electron Mobility, $cm^2\ V^{-1}\ sec^{-1}$	Sheet Electron Concentration, cm^{-2}	Apparent Electrical Activation, %
A	4000 ± 260	1950 ± 120	8×10^{11}	19
B	1340 ± 20	2520 ± 60	$(1.81 \pm 0.15) \times 10^{12}$	27 ± 2
C	730 ± 10	2710 ± 80	$(3.14 \pm 0.16) \times 10^{12}$	40 ± 2

The implant parameters are listed in Table 2.

Table 4. Electrical Properties of Be-Implanted Layers Annealed at 850°C for 30 min

Wafer	Sheet Resistivity, Ω/	Hole Mobility, $cm^2\ V^{-1}\ sec^{-1}$	Sheet Hole Concentration, cm^{-2}	Apparent Electrical Activation, %
A	5600 ± 250	180 ± 2	$(6.2 \pm 0.2) \times 10^{12}$	52 ± 2
B	4600 ± 60	200 ± 1	$(6.75 \pm 0.2) \times 10^{12}$	56 ± 2
C	4180 ± 170	206 ± 1.5	$(7.25 \pm 0.2) \times 10^{12}$	60 ± 2

The implant energy was 25 keV and the fluence used was $1.5 \times 10^{13}\ cm^{-2}$ The effective fluence was reduced to $1.2 \times 10^{13}\ cm^{-2}$ because of ions stopped in the oxynitride layer.

estimate, it is apparent that very high electrical activation has been achieved in all cases. The mobilities were in the expected range.

After eliminating diodes that were electrical shorts, the breakdown voltages of several diodes were estimated using a curve tracer. Wafers B and C were probed at random, and diodes with different diameters were measured. Figures 20 and 21 show histograms of the breakdown voltage of several diodes in wafers B and C, respectively. Diodes in wafer B appear to have breakdown voltages in the range of 20 to 30 V, while in wafer C most of the diodes exhibit breakdown voltages between 40 and 50 V. For the concentration of donors in the n-region of the device, the estimated breakdown should be between 20 to 30 V. Figures 22 through 25 show the I-V characteristics of several diodes from wafer C. Figures 23 and 24 show the I-V curves of diodes from wafer C. These diodes were 200 μm in diameter. The data were taken from diodes randomly selected on the wafer. The forward characteristics of the diodes can be expressed by the classical relation

$$I_f = I_o \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad .$$

The values of I_o and n are listed in Table 5. The ideality factor ($n \gtrsim 2$) clearly shows that the forward current is dominated by recombination in the space-charge region.

Using the data from wafer C, we have calculated the ratios of leakage currents at different bias voltages from a large number of 100- and 200-μm-diameter diodes. The data are listed in Table 6. The leakage current ratio varies from 2.12 to 3. The ratio of the area of the diodes is 4, while ratio of their perimeters is 2. It is thus clear that a substantial fraction of the leakage current results from surface leakage and is not a bulk phenomenon. Similarly processed devices with suitable guard structures should exhibit even lower leakage.

The I-V characteristics typical of devices in wafers A and B are shown in Figures 26 and 27, respectively. All diodes from wafer A exhibit higher leakage at all voltages. The reasons for this are not quite clear.

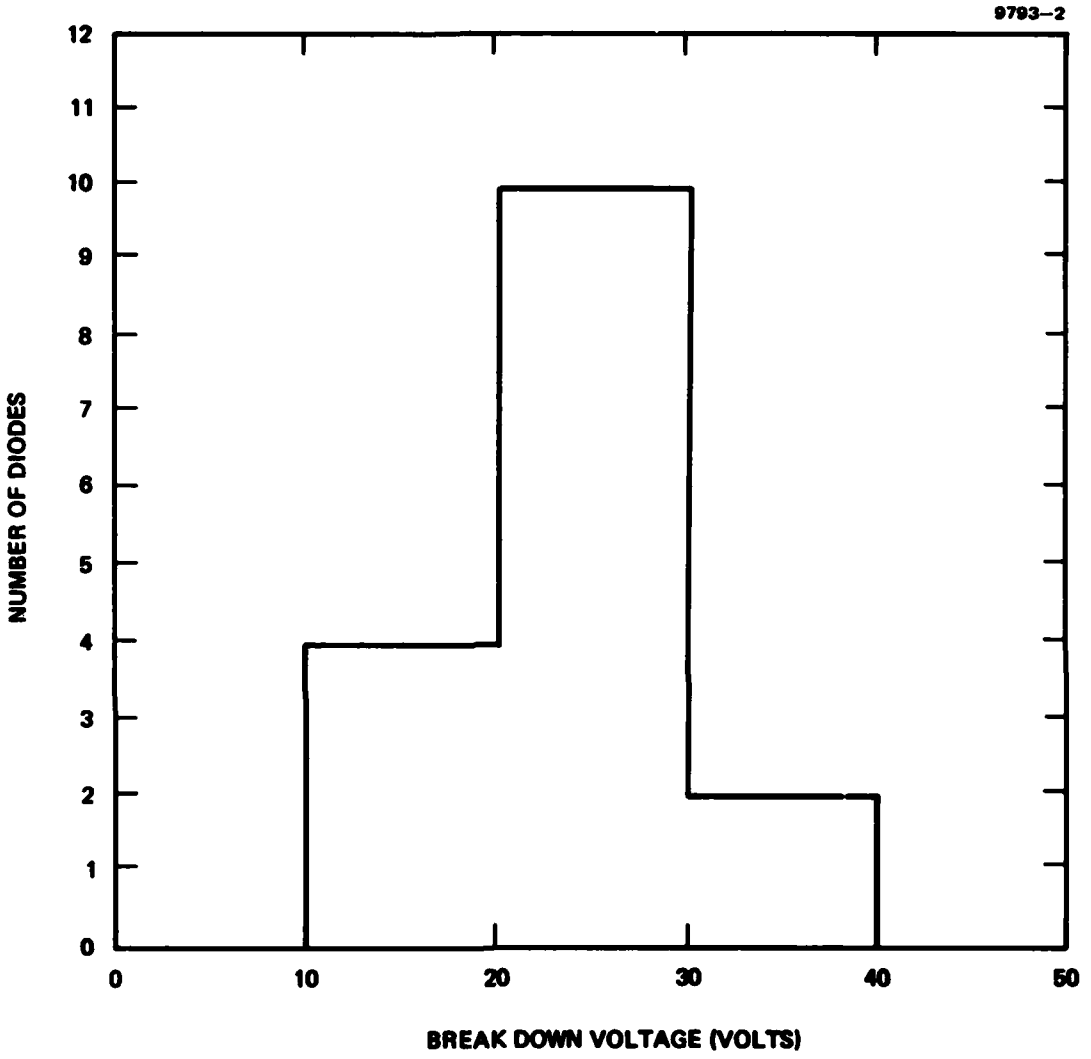

Figure 20. Distribution of breakdown voltage for typical diodes in wafer NRL-B.

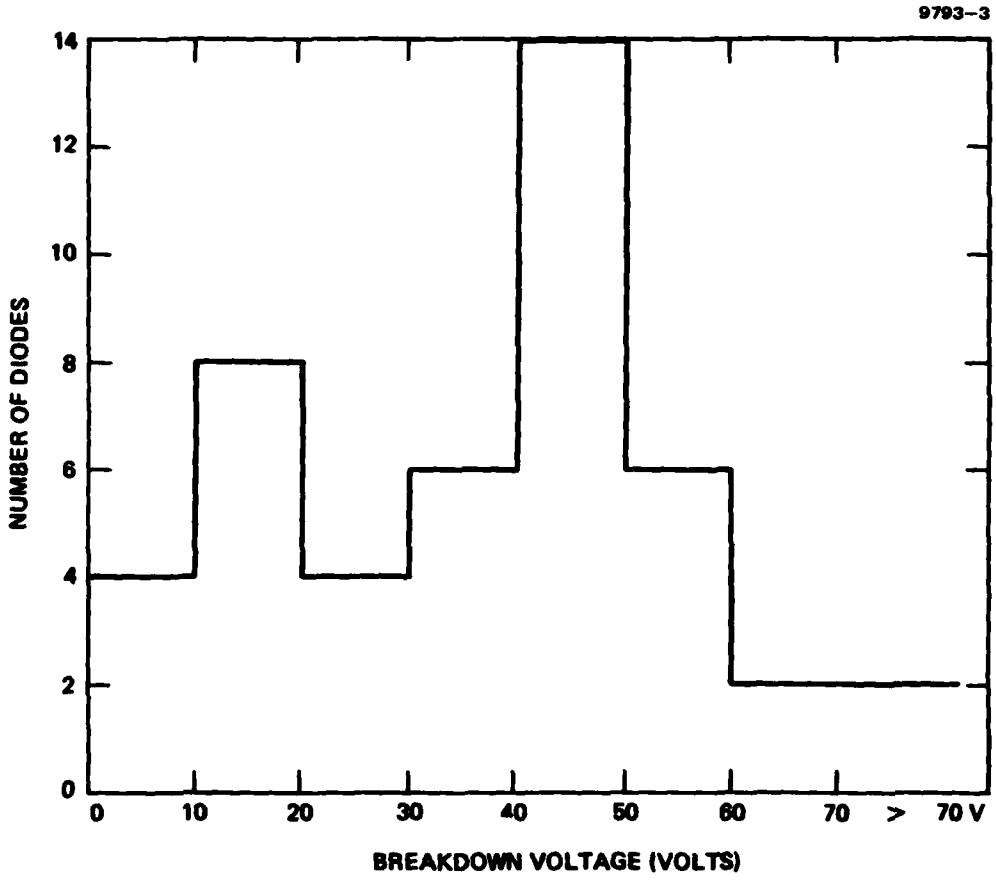

Figure 21. Distribution of breakdown voltage for typical diodes in wafer NRL-C.

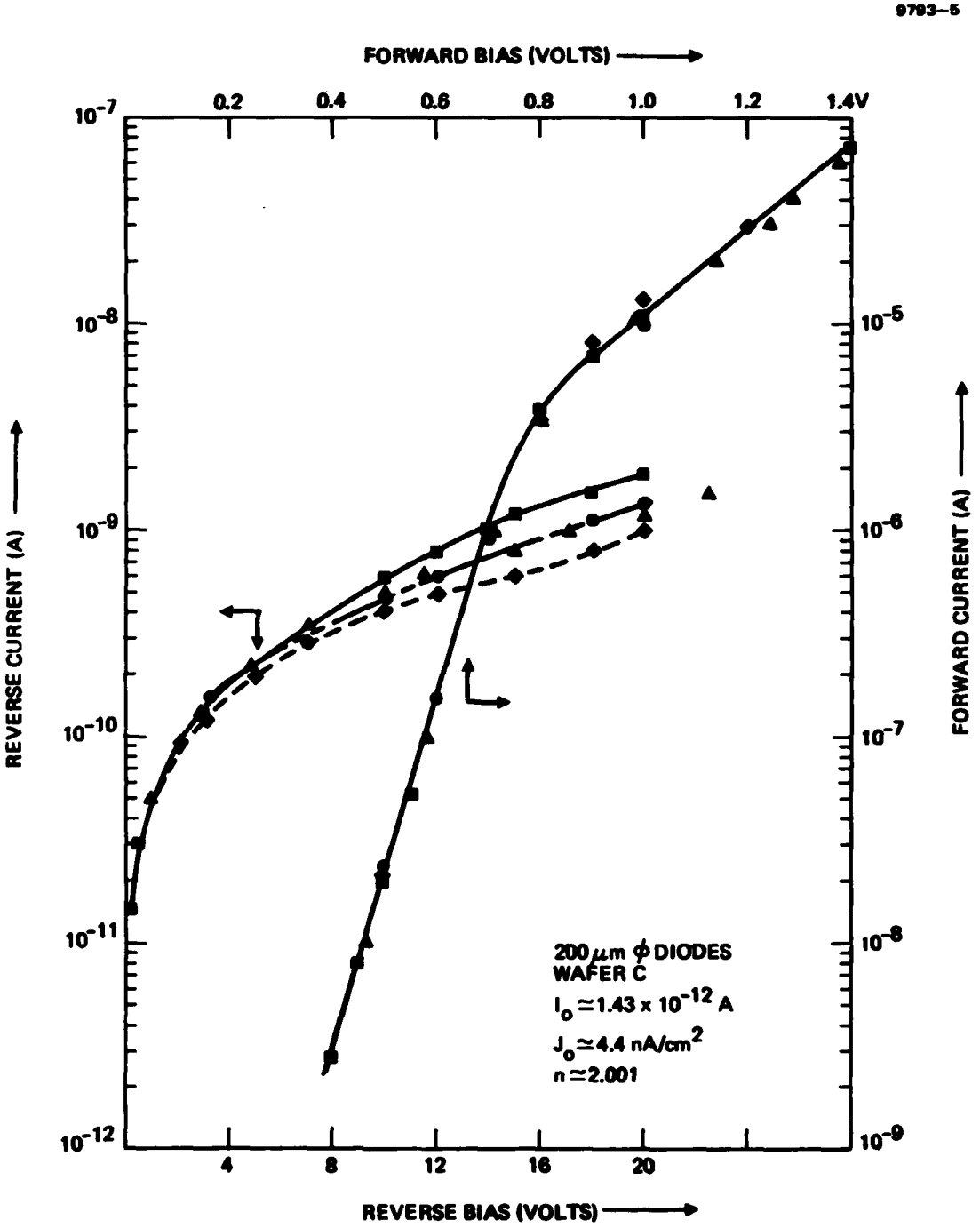

Figure 22. Current-voltage characteristics of 200-μm-diameter diodes from wafer NRL-C.

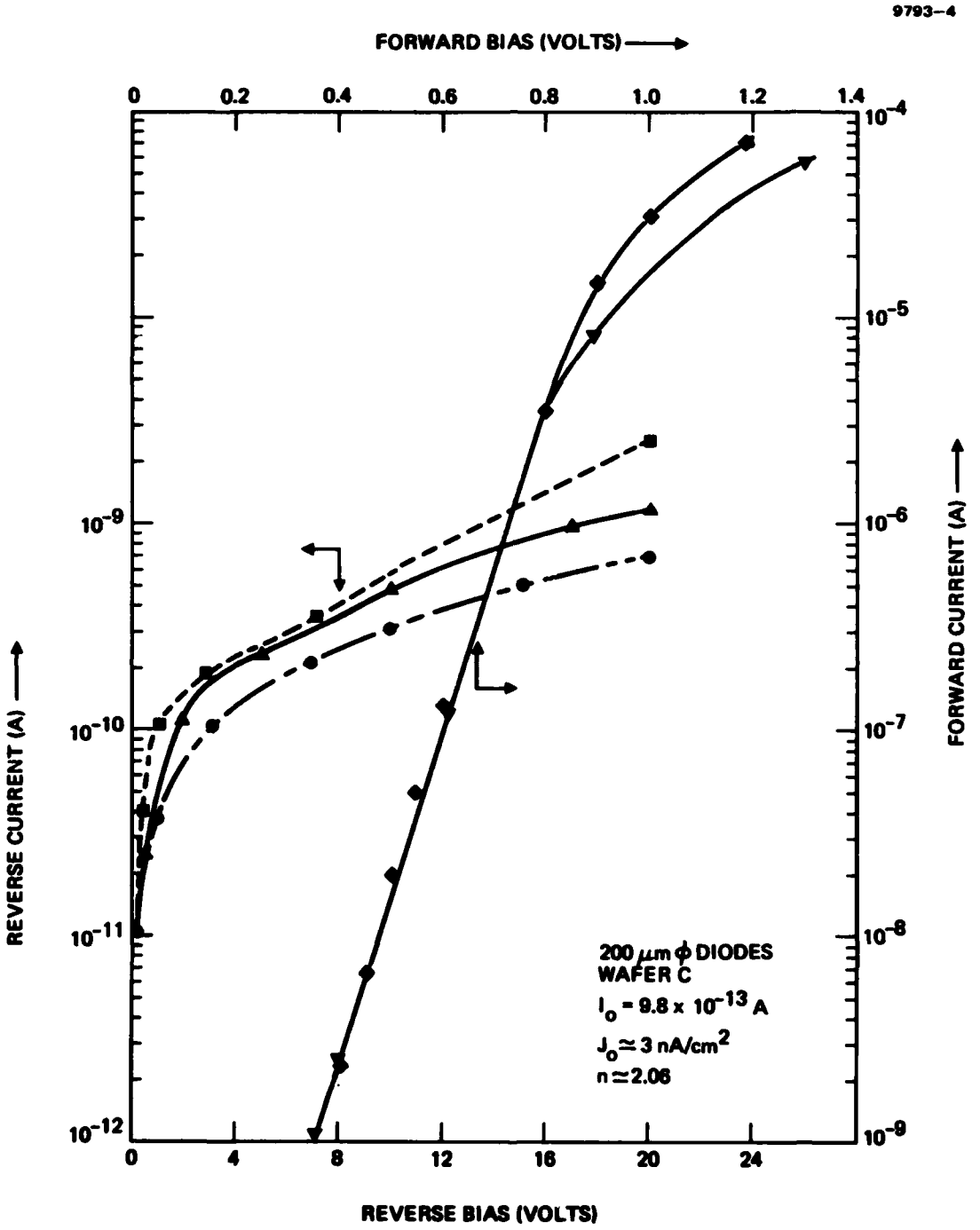

Figure 23. Current-voltage characteristics of 200-μm-diameter diodes from wafer NRL-C.

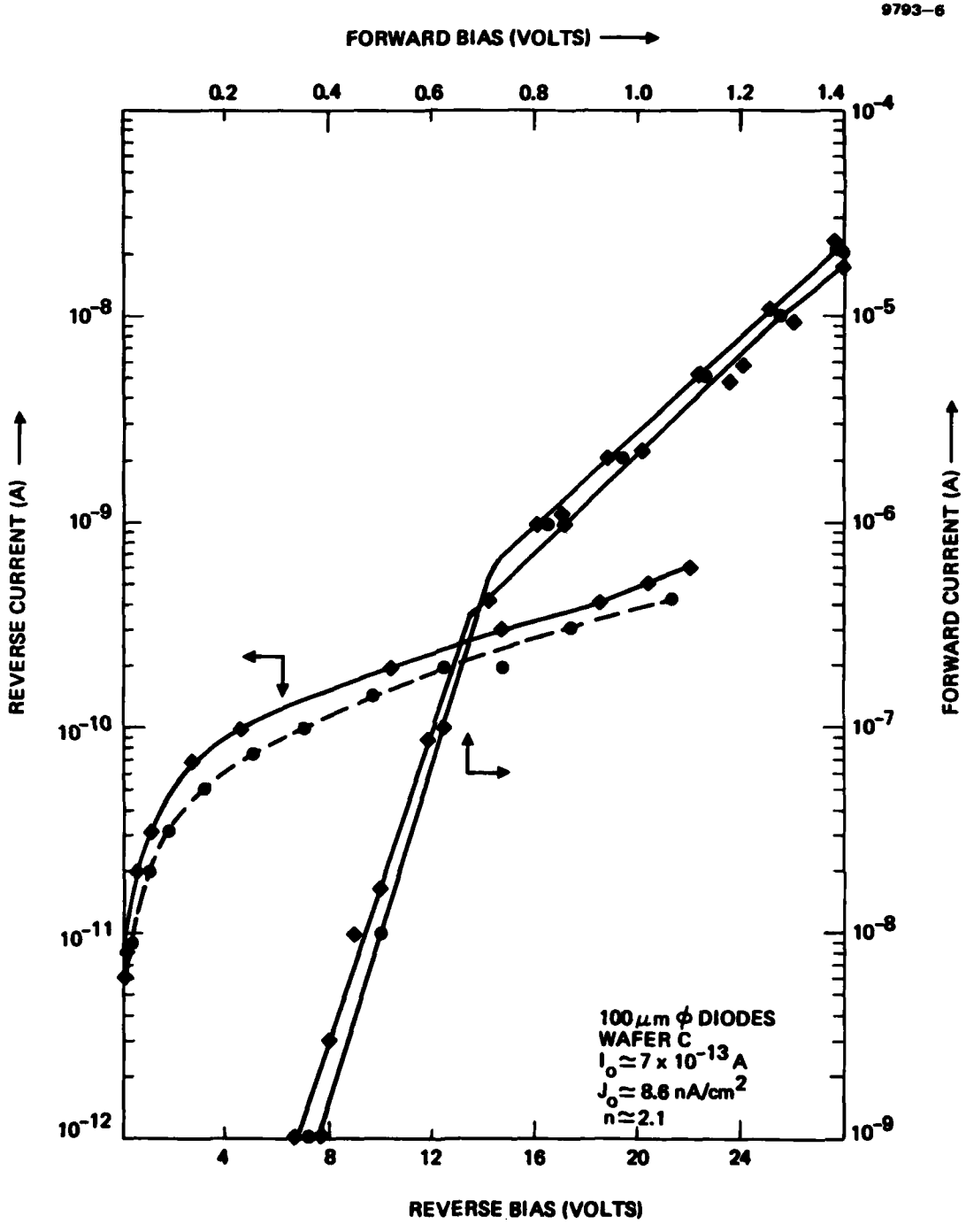

Figure 24. Current-voltage characteristics of 100-μm-diameter diodes from wafer NRL-C.

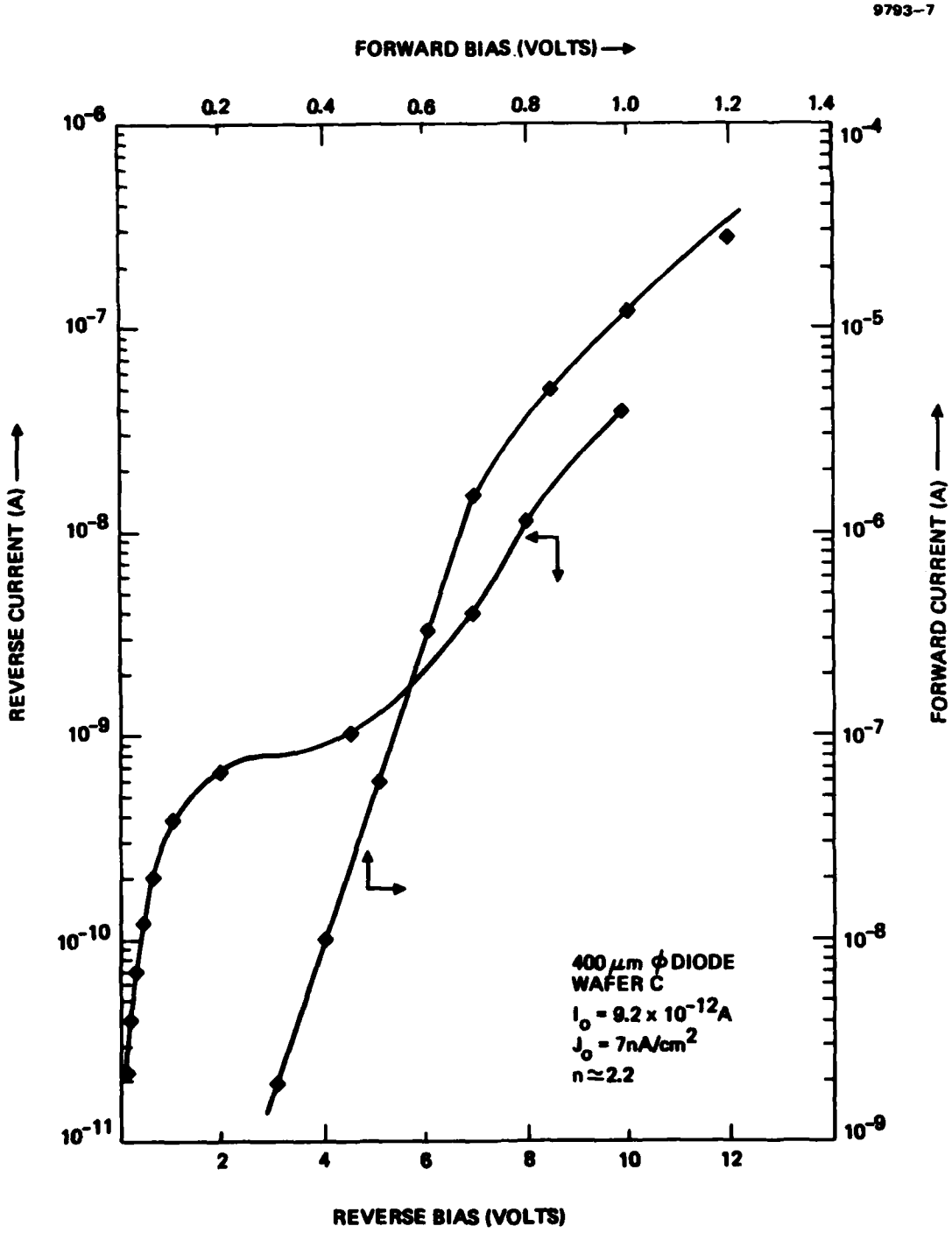

Figure 25. Current-voltage characteristics of 400-μm-diameter diodes from wafer NRL-C.

Table 5. Comparison of Diode Parameters Obtained from Sequentially Implanted GaAs p-n Junctions

Wafer	Diode Diameter, μm	I_o, A	n
A	400	4.3×10^{-11}	2.3
B	200	$(1 \pm 0.1) \times 10^{-12}$	(1.7 ± 0.2)
	400	$(1.45 \pm 0.05) \times 10^{-12}$	(2.002 ± 0.001)
C	200	$(8.5 \pm 1.5) \times 10^{-13}$	2.1 ± 0.02
	400	$(1.2 \pm 0.2) \times 10^{-12}$	2.03 ± 0.03
	800	$(9 \pm 4) \times 10^{-12}$	2.2 ± 0.1

Table 6. Comparison of Leakage Currents from Diodes in Wafer C for Various Applied Reverse Bias Voltages

Bias Voltage, V	Diode Diameter, μm	Ratio of Areas	Average Leakage Current, A	$\frac{I_L \text{ (200 μm } \phi)}{I_L \text{ (100 μm } \phi)}$
1	200	4	$(2.33 \pm 0.47) \times 10^{-11}$	2.12 ± 0.69
	400		$(4.95 \pm 1.26) \times 10^{-11}$	
2	200	4	$(3.7 \pm 0.8) \times 10^{-11}$	2.75 ± 0.94
	400		$(10.2 \pm 2.7) \times 10^{-11}$	
5	200	4	$(8.2 \pm 1.15) \times 10^{-11}$	2.6 ± 0.52
	400		$(21.3 \pm 3) \times 10^{-11}$	
10	200	4	$(1.6 \pm 0.12) \times 10^{-10}$	3 ± 0.64
	400		$(4.8 \pm 0.96) \times 10^{-10}$	
15	200	4	$(2.675 \pm 0.3) \times 10^{-10}$	2.8 ± 0.5
	400		$(7.5 \pm 1.05) \times 10^{-10}$	
18	200	4	$(3.23 \pm 0.41) \times 10^{-10}$	2.55 ± 0.6
	400		$(8.25 \pm 1.92) \times 10^{-10}$	
20	200	4	$(3.83 \pm 0.6) \times 10^{-10}$	2.82 ± 0.7
	400		$(10.8 \pm 2.1) \times 10^{-10}$	

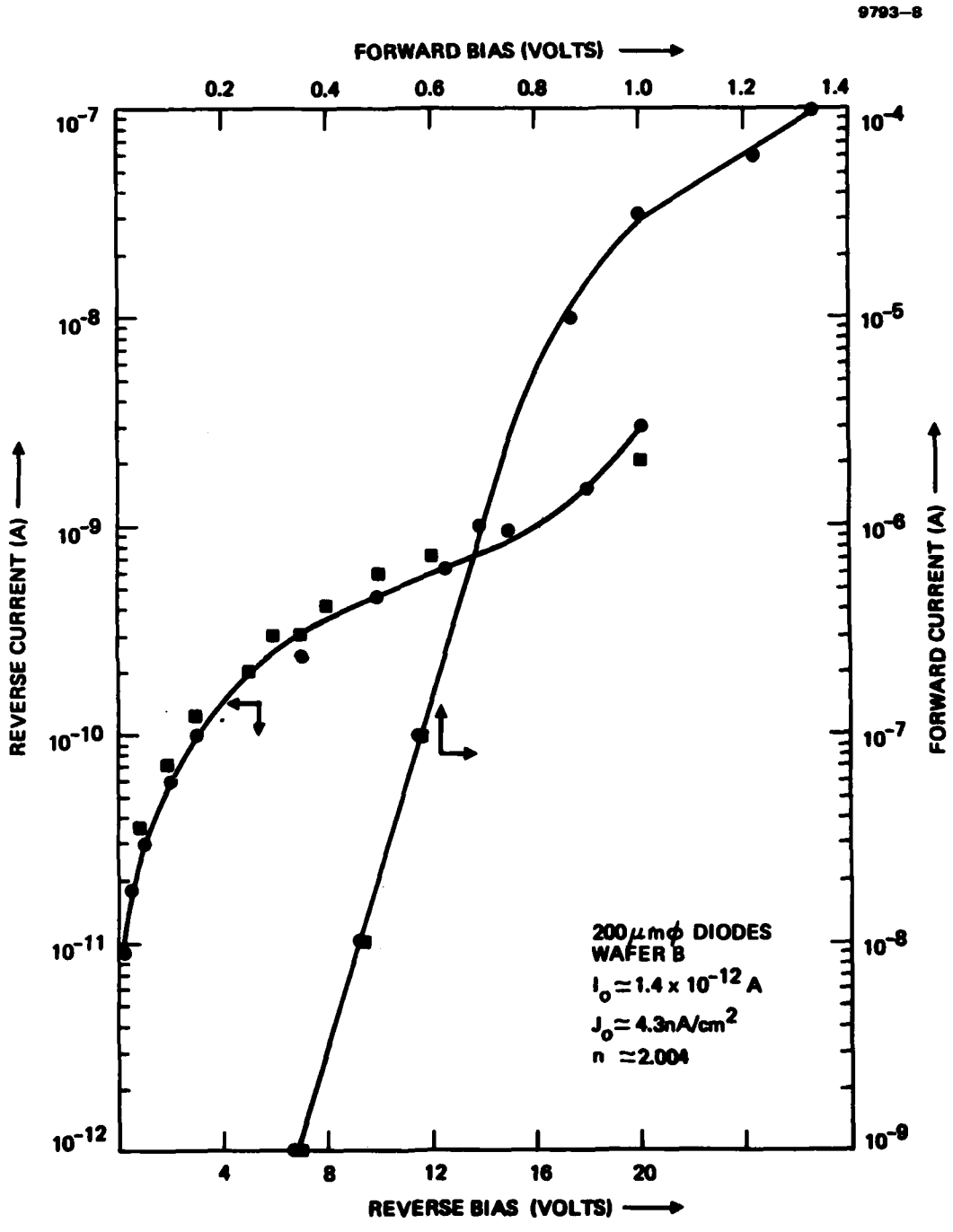

Figure 26. Current-voltage characteristics of 200-μm diameter diodes from wafer NRL-A.

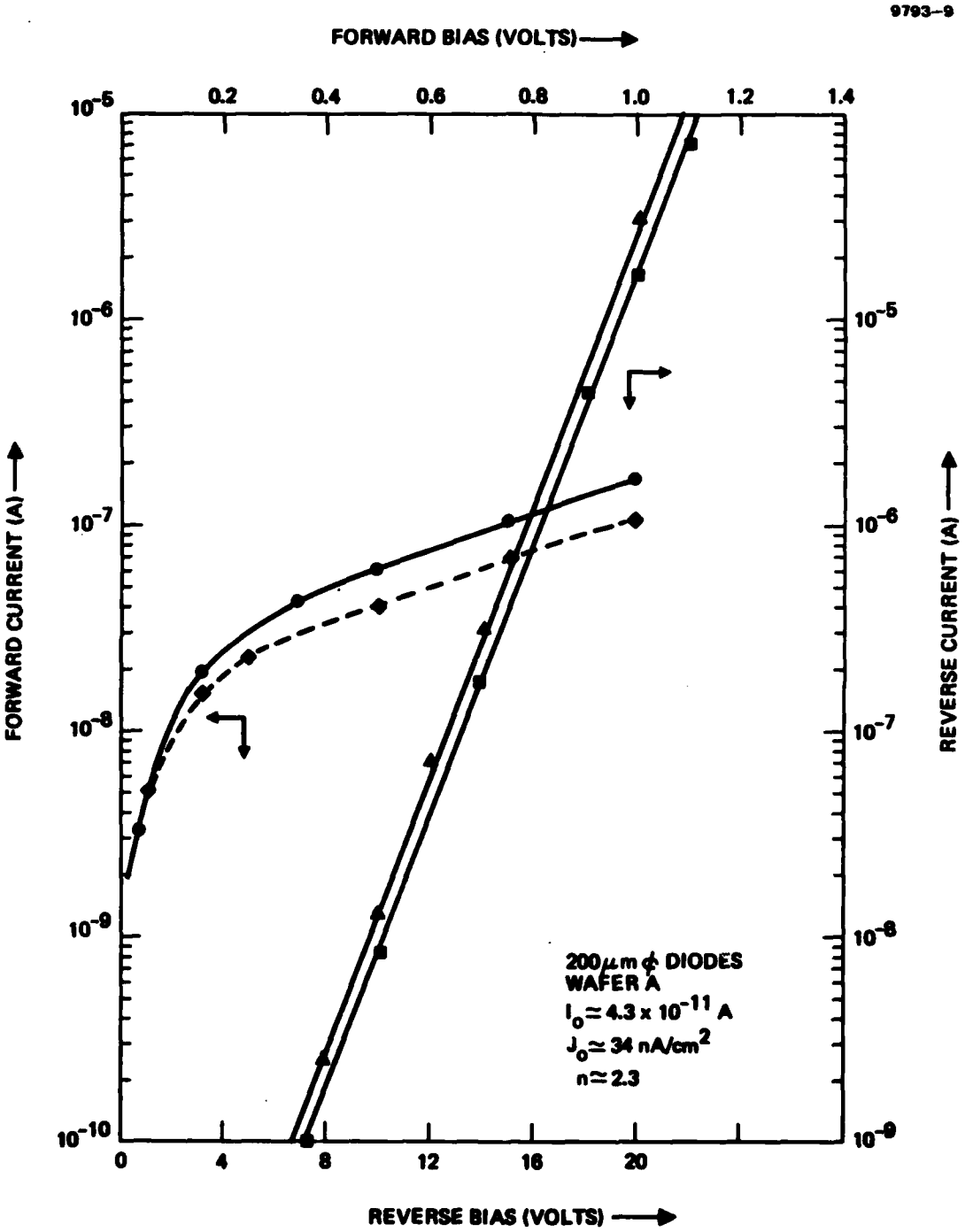

Figure 27. Current-voltage characteristics of 200-μm-diameter diodes from wafer NRL-B.

In conclusion, the electrical evaluation studies clearly show that low-leakage, planar, isolated p-n junctions exhibiting reasonable breakdown voltages can be fabricated by sequential ion implantation in semi-insulating GaAs.

REFERENCES

1. W.V. McLevige, M.J. Helic, K.V. Vaidyanathan, and B.G. Streetman, J. Appl. Phys. 48, 3342 (1977) and references there in.

2. C.L. Anderson, K.V. Vaidyanathan, H.L. Dumlap and G.S. Kamath, J. Electrochem. Soc., 127, 925 (1980).

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